INDIRECT MINIMIZATION OF COMMON-MODE VOLTAGE WITH FINITE CONTROL-SET MODEL PREDICTIVE CONTROL IN A FIVE-LEVEL INVERTER

By

Dharmikkumar Prajapati

Presented to Lakehead University
in partial fulfillment of the
requirements for the degree of
Master of Science
in the Program of
Electrical and Computer Engineering

Lakehead University
April 2024

Thunder Bay, Ontario, Canada, 2024

ABSTRACT

Multilevel inverters (MLIs) are counted as the crucial part of the electric drive systems (EDSs) primarily due to their ability to handle higher operating powers and voltages, to provide high-quality output waveform, and to reduce dv/dt. Nevertheless, MLIs require a complex control system to handle multiple control objectives such as load currents, floating capacitors (FCs) voltage, current tracking errors, and common-mode voltage (CMV) minimization. Among them, the load current and FC voltage objectives are associated with the basic operation of the MLI, whereas the CMV minimization is associated with the safety and reliability of the MLI-fed EDSs. Hence, the CMV minimization becomes obligatory to ensure the safety of the system.

To achieve multiple objectives of MLIs, finite control-set model predictive control (FCS-MPC) methods became promising solutions due to the following features: (i) ease of implementation, (ii) intuitive philosophy, (iii) fast transient response, (iv) ability to handle multiple objectives with a single cost function, (v) easy to compensate control delay, and (vi) flexible to include system constraints and nonlinearities. However, FCS-MPC methods use a cost function with weighting factor to directly minimize the CMV of MLIs. The improper selection of weighting factors directly affects the current harmonic distortion of MLIs. They also need higher execution time to implement in real-time control platforms.

To address the challenges associated with the conventional FCS-MPC methods, a new per-phase FCS-MPC philosophy is proposed in this thesis. The proposed philosophy minimizes the CMV without using a cost function, thereby eliminating the need of weighting factors and their impact on current harmonic distortion. Also, the proposed FCS-MPC is designed to achieve the control objectives of each phase by using an independent cost function, resulting in a shorter execution time. The proposed philosophy is applied to a five-level inverter (FLI). The continuous-time and discrete-time models of FLI are developed to implement the proposed FCS-MPC. Finally, the steady-state and transient performances are verified on dSPACE-DS1103 controlled FLI laboratory prototype. Also, a comparative analysis of the proposed and conventional FCS-MPC is presented.

ACKNOWLEDGEMENTS

I would like to express a deep sense of gratitude and whole-hearted thanks to my supervisor, Dr. Apparao Dekka for his invaluable guidance and unwavering support throughout the course of my research work. It has been a genuine privilege to have worked with him, and I am very grateful that I have pursued my Master's studies under his excellent supervision.

I would like to extend another thank you to my colleague, Mr. Hoang Le, for his tireless efforts in assisting me with the preparation and execution of laboratory experiments. It is without a doubt that, Mr. Hoang Le and Dr. Apparao Dekka's help, these experiments could not have been completed as quickly as seamlessly as they were.

I am highly obliged to my parents for their unconditional assistance and lucid guidance cannot be depicted by words, particularly in my periods of hardships and difficulties. Special thanks to my dear friends Priyansh Gupta, and Aira Angelika Reyes who helped me in tough times and provided me with encouraging words to achieve my goals. Without their help, the completion of my studies may not have been possible.

Additionally, I would like to give special thanks to Drs. Ameli and Wei for raising some excellent points that have helped me improve the overall quality of my research work. Their insights and suggestions have been invaluable, and I am deeply appreciative of their time and efforts.

Finally, I would like to acknowledge all the financial support from Dr. Apparao Dekka.

Contents

List of Figures

List of Tables

LIST OF ACRONYMS

AC	Alternating Current
CM	Common-Mode
CMT	Common-Mode Transformer
CMV	Common-Mode Voltage
DC	Direct Current
DM	Differential-Mode
EDS	Electric Drive System
FC	Floating Capacitor
FCS-MPC	Finite Control-Set Model Predictive Control
FLI	Five-Level Inverter
HVDC	High-Voltage Direct-Current
IGBT	Insulated-Gate Bipolar Transistor
kV	Kilovolt
MLI	Multilevel Inverter
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MPC	Model Predictive Control
MV	Medium-Voltage
MW	Megawatt
PI	Proportional-Integral
PWM	Pulse-Width Modulation
SMPC	Sequential Model Predictive Control
SVM	Space Vector Modulation
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
VSC	Voltage Source Converter
VSI	Voltage Source Inverter
VSR	Voltage Source Rectifier

LIST OF SYMBOLS

Superscript

$\widehat{\ }$	Peak quantity
$*$	Reference quantity
p	Effective value of the predicted quantity
pe	Resultant value of the predicted quantity

Subscript

$x \in \{p, q, r\}$	AC output phases
k	Capacitor index number
i	Quantity related to current
v	Quantity related to voltage

System Quantities

S_{gr}	Inverter rated power (W)
V_{gr}	Inverter rated voltage (V)
I_{gr}	Inverter rated current (A)
f_{gr}	Inverter rated frequency (Hz)
I_g^*	Fundamental reference current (A)
f_g^*	Fundamental reference frequency (Hz)
θ_o	Three-phase system phase angle difference

Voltage and Current Quantities

V_{dc}	DC-link voltage (V)
v_{C1x}, v_{C2x}	Floating capacitor voltage in phase-x (V)
v_{pq}, v_{qr}, v_{rp}	Three-phase line-to-line voltages (V)
v_{cmr}	Rectifier common-mode voltage (V)
v_{cmi}	Inverter common-mode voltage (V)
v_{xm}	Inverter AC voltage of phase-x (V)
v_{nm}	Common-mode voltage of the FLI (V)
v_{xn}	Inverter load voltage of phase-x (V)
v_{cm}	Common-mode voltage of the EDS (V)
i_x	Inverter AC current of phase-x (A)
i_{C1x}, i_{C2x}	Floating capacitor currents in phase-x (A)

Passive Elements

L_x	Load inductor of phase-x (H)
L_{dm}, L_f	Filter inductance (H)
R_x	Load resistor of phase-x (Ω)
R_{cm}	Common-mode resistor (Ω)
C_m	Motor parasitic capacitance (F)
C_t	Transformer parasitic capacitance (F)
C_g	Grid parasitic capacitance (F)
C_{dm}, C_f	Filter capacitance (F)
C_{x1}, C_{x2}	Floating capacitor capacitance of phase-x (F)

LIST OF PUBLICATIONS

[1] **D. Prajapati**, A. Dekka, D. Ronanki, and J. Rodriguez, "Low-Complexity Heun's Method-Based FCS-MPC With Reduced Common-Mode Voltage for a Five-Level Inverter," in *IEEE Transactions on Power Electronics*, vol. 39, no. 3, pp. 3329-3338, March 2024, doi: 10.1109/TPEL.2023.3342756.

Chapter 1

INTRODUCTION

Over the past decade, multilevel inverters (MLIs) have become one of the promising solutions for high-power and medium-voltage (MV) industrial applications [1, 2], owing to their features of low harmonic distortion, low dv/dt, low switching losses, and low device voltage stress [3]. Over the course of more than three decades of research and development, several multilevel inverter (MLI) topologies have been developed, and they are categorized into integrated MLIs and multi-cell inverters [2]. Typically, integrated MLIs are designed to handle operating voltages from 2.3 kV to 4.16 kV, whereas the multi-cell inverters can reach more than 6 kV operating voltage [4, 5]. These inverters have successfully commercialized as both standard and customized products that support a variety of applications, including electric drive systems (EDSs) [6, 7], wind energy conversion systems [8], photovoltaic energy systems [9], high-voltage direct current (HVDC) transmission systems [10, 11], power quality devices [12, 13], electric vehicles [14], railway traction systems [15, 16], and marine power systems [17].

Irrespective of the MLI topology, it requires a complex control system to handle multiple control objectives. These objectives are further categorized into load and inverter objectives [18], and they vary with the type of MLI topology and type of application. Some of the

load objectives are currents, torque/flux (for EDS applications), and active/reactive powers (for grid applications), and these objectives directly related to the operation of the MLI. On the other hand, the converter objectives directly affect the reliability of the MLI. Some of the converter objectives are floating capacitor (FC) voltages, switching frequency/losses minimization, and common-mode voltage (CMV) minimization [19]. Among them, CMV is one of the critical issue in MLIs, which induces bearing currents and shaft voltages in EDSs, and causes premature bearings failures and shaft breakdown over a long run [20–22]. This further leads to increased cost of maintenance and downtime. Hence, CMV minimization is critical to develop a reliable MLI-fed EDSs.

1.1 Background and Motivation

Over the years, the impact of CMV on MLI-fed EDSs has been rigorously investigated and developed several solutions to either block or minimize the CMV [23]. These solutions have been broadly categorized into hardware-based [24, 25] and software-based solutions [26, 27]. The hardware-based solutions need an additional hardware circuitry to be installed in the EDSs to block or minimize the CMV. Some of the hardware-based solutions are the use of isolation transformers [28, 29], common-mode filters/chokes [30–34], common-mode transformers [35–37], and fourth arm converter approach [38]. These solutions are highly effective in blocking or minimizing the CMV. However, they need additional space to install them, which leads to increase in the size and cost of the overall MLI-fed EDSs.

On the other hand, the software-based solutions are widely studied for minimizing CMV in MLI-fed EDSs. These solutions mainly involve simple modifications and implementation of control algorithms in digital control platforms [26, 27]. Hence, these solutions significantly reduce the hardware complexity, volume, and cost of the EDSs. Some of the popular software-based solutions are linear control methods with space vector modulation (SVM) scheme [26,

39], sequential model predictive control (SMPC) methods [40,41], and finite control-set model predictive control (FCS-MPC) methods [27]. In linear control methods, the space vector modulation scheme is designed to switch the MLIs with the selective switching vectors that produce the lowest CMV [42, 43]. However, the real-time selection of such switching vectors from all the redundancy switching vectors is quite complex as it involves sector identification, duty cycles calculation, and switching sequence formulation [44]. Moreover, the available redundancy switching vectors drastically increases with the output levels of MLIs. Hence, these methods are difficult to apply for higher output level MLIs [45]. Furthermore, the linear controller method uses synchronous dq-frame PI-regulators to control the currents and logical functions-based algorithm to balance the FC voltages. These methods exhibit poor transient response due to the limited controller bandwidth, improper selection of PI-gains, and switching frequency [46, 47].

Alternatively, SMPC methods allow flexible control of multiple objectives in MLIs by using multi-stage optimization process [40,41,48,49]. These methods follow the space vector philosophy in identifying the candidate switching vectors for optimization process [40, 48]. Furthermore, it requires a weighting factor dependent cost function to minimize the CMV, which affects the MLIs performance. On the other hand, the offline selection of switching vectors with the lowest CMV has been applied in selecting the candidate switching vectors for optimization process [41, 49]. This process becomes cumbersome with the increases in output levels of MLIs. Irrespective of the SMPC method, they takes shorter execution time and exhibit poor transient performance compared with FCS-MPC methods [50].

FCS-MPC methods use single cost function to achieve multiple objectives of MLIs, while following the intuitive philosophy in their implementation [51]. However, the performance of FCS-MPC methods greatly depends on the discrete-time models accuracy and selection of weighting factors [52]. Traditionally, the forward Euler integration method-based models

are employed in implementation of FCS-MPC methods [53]. These models lead to higher current tracking error and switching frequency under a larger sampling time operation [54]. Alternatively, Heun's integration method-based models are adopted in the implementation of FCS-MPC methods. These models improve the MLI performance while operating at a low switching frequency. However, they need a longer execution time to implement in real-time controllers [55]. Irrespective of the use of forward Euler and Heun's method-based models, the conventional FCS-MPC methods need a cost function with weighting factor to directly minimize the CMV in MLIs [56, 57]. Moreover, the selection of weighting factors directly affect the MLI performance, including current harmonic distortion and FC voltage ripple [58]. Hence, there is a need for FCS-MPC methods, which can take a shorter execution time while minimizing the CMV in MLIs without using a weighting factor dependent cost function.

1.2 Objectives of the Thesis

Aforementioned issues and challenges associated with the conventional FCS-MPC methods for MLIs are addressed in this thesis. The objectives of this thesis are summarized as follows:

- Developing an FCS-MPC method to minimize the CMV in MLIs without using a weighting factor dependent cost function.
- Developing an FCS-MPC method that takes a shorter execution time to implement in real-time controllers for MLIs.
- Developing Heun's integration method-based discrete-time models of five-level inverter to implement the proposed FCS-MPC philosophy.
- Conducting experimental studies to verify the effectiveness of the proposed FCS-MPC.

- Conducting a comprehensive comparison of the proposed and conventional FCS-MPC methods.

1.3 Outline of the Thesis

The outline of the thesis is as follows: Chapter 2 presents a comprehensive review of various hardware-based and software-based solutions for CMV minimization in MLIs. Chapter 3 presents the implementation and validation of the proposed FCS-MPC methodology for an FLI. This chapter also presents the experimental performance at different operating scenarios, including a comprehensive comparison with the conventional FCS-MPC method. Chapter 4 outlines the conclusions and the future work of this research.

Chapter 2

OVERVIEW OF COMMON-MODE VOLTAGE MINIMIZATION METHODS

2.1 Introduction

Due to the switching actions of the switching devices, the multilevel inverters (MLIs) produce a common-mode voltage (CMV). The representation of CMV in voltage source converter (VSC) fed electric drive systems (EDSs) is depicted in Fig. 2.1 [7]. The EDSs consist of a voltage source rectifier (VSR) to convert the fixed AC power from medium-voltage (MV) grid to DC power, whereas the DC power is converted into variable AC power on the MV motor-side by using a voltage source inverter (VSI). The VSR and VSI produces CMV, and they are denoted with v_{cmr} and v_{cmi}, respectively [7]. The net CMV (v_{cm}) of the EDSs is equal to the summation of v_{cmr} and v_{cmi}, and it measured between the AC-grid and motor grounds as shown in Fig. 2.1. The differential-mode (DM) filter on grid and motor-sides mainly improves the harmonic performance on their respective sides, and does not have any impact on the CMV [7]. These filters can be eliminated if the EDSs are fed by MLIs rather than two-level VSR/VSI.

The produced CMV component in MLI-fed EDSs superimposes on the load voltage component, resulting in a premature failure of motor winding insulation [34, 59]. Also, the

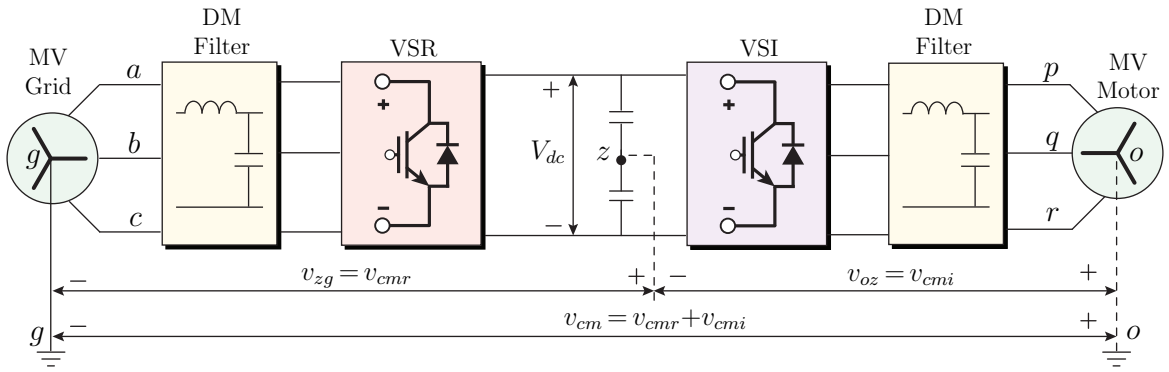


Figure 2.1: Common-mode voltage representation in EDSs.

CMV induces bearing currents and shaft voltages through stray capacitance between motor frame and bearings in EDSs, which causes bearing failure and shaft breakdown over a long run [20,21]. As a result, the EDSs reliability and life expectancy becomes shortened. Hence, the CMV minimization of CMV is very critical in developing a reliable MLI-fed EDSs.

Over the years, several solutions have been developed to block or minimize the CMV in MLIs and their applications. These solutions are broadly categorized into hardware-based solutions and software-based solutions in this thesis. The hardware-based solutions use external hardware circuitry to block or minimize the CMV in MLIs. Some of the hardware-based solutions are isolation transformers [28, 29], common-mode (CM) filters [30–33], common-mode transformer (CMT) [35–37], and fourth-leg converter structures [38]. On the other hand, software-based involves simple modifications and implementation of control algorithms. Some of the software-based solutions are linear controllers with space vector modulation (SVM) scheme [26, 39, 42, 44, 45, 60, 61], sequential model predictive control (SMPC) methods [40,41,48,49], and finite control-set model predictive control methods [27,53,56,57]. This chapter delves into both hardware-based and software-based solutions for the minimization of CMV in MLIs. Also, the advantages and problems associated with these solutions are highlighted in this chapter.

2.2 Hardware-Based CMV Minimization Approaches

Hardware-based solutions encompass a range of techniques and methodologies aimed at reducing or blocking CMVs in MLIs. These solutions typically involve the use of specialized components, circuit designs, and shielding methods to suppress CMVs effectively in MLIs.

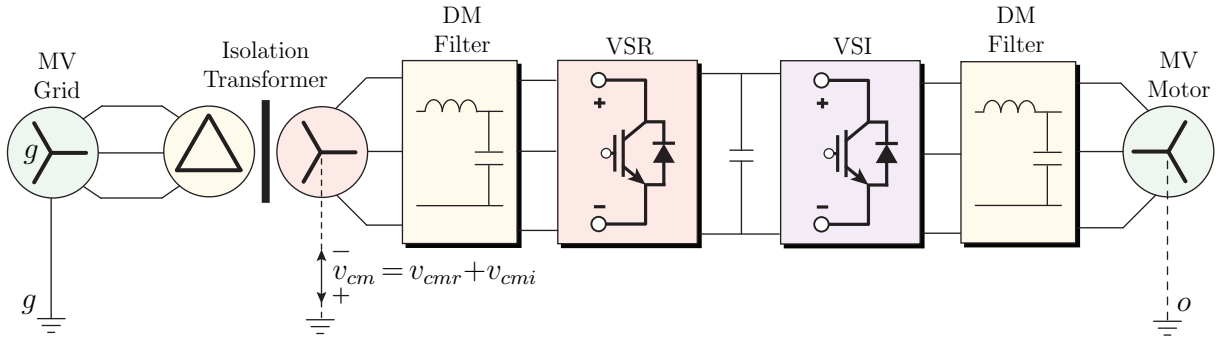


Figure 2.2: CMV blocking with isolation transformer.

2.2.1 Isolation Transformer Approach

Traditionally, the isolation transformer is used to block the CMV in MLI-fed EDSs, and it is incorporated on AC-grid side of the EDSs as shown in Fig. 2.2 [7,28]. In high-power applications, the isolation transformer is designed with phase-shifted multiple secondary windings (12-pulse or 18-pulse transformers) to improve the grid-side harmonic performance [29]. Typically, the delta-winding configuration of the isolation transformer is connected to AC-grid side, whereas the Y-winding configuration is connected to the VSR as shown in Fig. 2.2. The delta winding of the transformer blocks the common-mode current entering from the grid to the motor side. Moreover, the grid and motor neutrals are grounded. Hence, the motor CMV appears between the transformer Y-winding neutral and ground point as shown in Fig. 2.2. Overall, the use of isolation transformer does not eliminate the motor CMV, and it is simply transfers the CMV from motor to the transformer. Therefore, the transformer winding insulation should be designed to withstand the additional CMV voltage stress [7,28].

However, the motor stator winding neutral is not accessible in practice. In such scenario, the motor and transformer neutrals were left floating as shown in Fig. 2.3 [7, 28]. In that case, the CMV distribution between the transformer and motor depends on the size of the transformer and motor parasitic capacitances of C_t and C_m, respectively as shown in Fig. 2.3. These capacitances also referred as a common-mode (CM) capacitance as they provide path for the CM current produced the CMV [7, 28]. Typically, the size of C_m is much larger than the C_t, resulting in a significant amount of CMV appears between the transformer neutral to ground. Therefore, the CMV seen by the motor is very small, which leads to improvement in motor reliability and life expectancy.

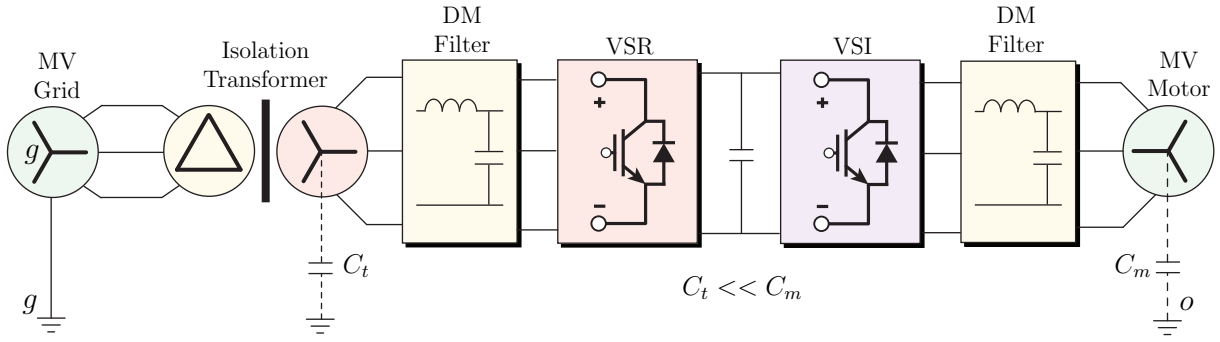


Figure 2.3: CMV blocking with isolation transformer including parasitic capacitance.

The isolation transformer effectively blocks the CMV for the motor, but it has several drawbacks [7, 28]:

- **Size and Weight**: Isolation transformers are often bulky and heavy, especially for high-power applications. Integrating them into electric drives may required additional space and structural support, which can be impractical in some cases.

- **Cost**: Isolation transformers can be relatively expensive compared to the CMV mitigation techniques. The cost of the transformer itself, along with installation and maintenance expenses, can add to the overall system cost.

- **Energy Losses**: Isolation transformer incur energy losses due to electrical and magnetic losses. These losses contribute to reduced efficiency and may required additional cooling measures to dissipate heat effectively.

2.2.2 Common-Mode Filters

The passive common-mode (CM) filters are one of the feasible solutions to mitigate the CMV in MLI-fed EDSs, and they are designed with the passive components such as resistor, capacitor, and inductor [32, 62]. Typically, a large CM inductor is used as a CM filter in EDSs [24], and it is referred to as a passive CM filter. The circuit configuration of a passive CM filter is shown in Fig. 2.4 [30]. Typically, the CM inductor has been integrated with the DM filter to reduce the overall size of the CM filter. In which, the DM filter is designed to eliminate the ripple in motor or grid currents, whereas the CM inductor blocks the CMV and suppress the CM current in MLI-fed EDSs [30]. Furthermore, the CM resistance will be included in the CM current path to damp the resonance oscillations caused by the DM filter as shown in Fig. 2.4. Depending on the EDSs structure, the CM inductor can be installed on grid-side, motor-side or DC-link side [30–32, 63, 64].

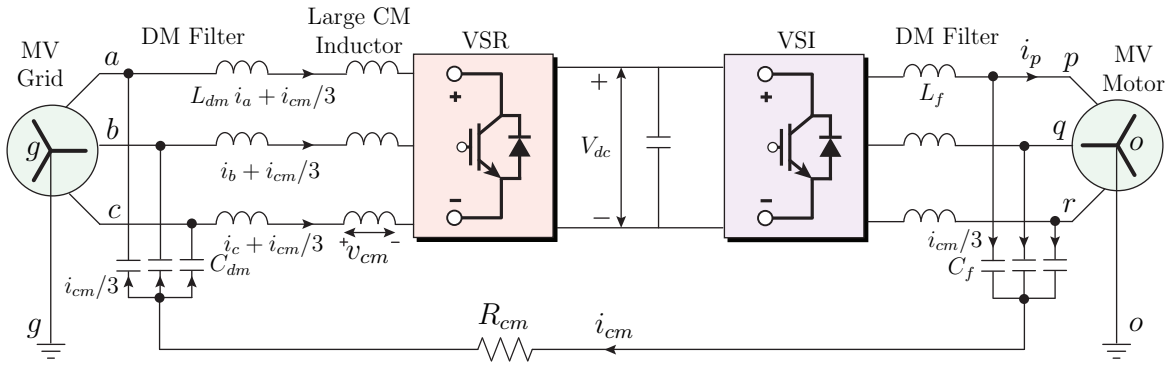


Figure 2.4: MLI-fed EDSs with passive common-mode filter

However, the use of passive CM filters lead to additional energy losses, resulting in a reduction in the system efficiency. These filters together with line inductances will cause

resonance problems, which will affect the converter reliability. Also, the use of passive CM filters increase the overall system weight, volume, and cost [30–32, 63].

Alternatively, the active CM filters have been investigated for minimizing the CMV in MLIs-fed EDSs [33, 65], and the typical configuration of active CM filter is shown in Fig. 2.5 [33]. The active CM filters are normally designed with power electronic converters together with passive components as shown in Fig. 2.5. Typically, these filters are designed to inject a CM current with opposite phase into the main circuit, resulting in complete elimination of CM current and CMV from the EDSs [33]. However, the performance of active CM filters greatly depends on accuracy of feedback measurement circuits and closed-loop controllers bandwidth [33,65]. Additionally, the cost and power losses are key challenges in active CM filters.

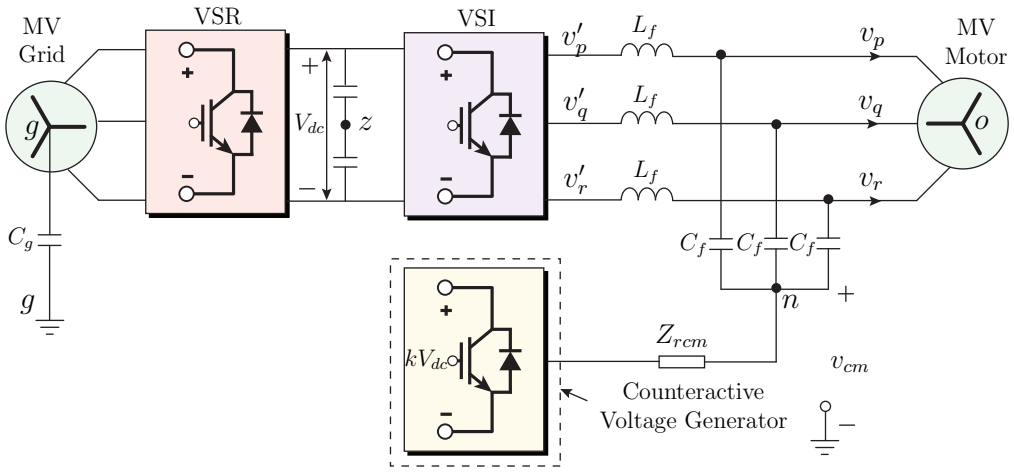


Figure 2.5: MLI-fed EDSs with active common-mode filter.

2.2.3 Common-Mode Transformers

The conventional passive CM filters cannot eliminate the CMV completely, and they require a large CM inductor to block the CMV. To improve the performance of passive CM filter, a new passive filter circuit based on common-mode transformer (CMT) is presented,

and its circuit configuration is shown in Fig. 2.6 [37]. The new filter circuit achieves the reduction or complete elimination of CMV in EDSs through combining CMT and *RLC* filter components as depicted in Fig. 2.6. The *RLC* filter is designed to suppress the DM dv/dt. Additionally, it acts as a low-pass filter and trap the CM current entering into the EDSs as shown in Fig. 2.6. The trapped CM current pass through the primary winding of the CMT and induces a voltage component corresponding to the CM current. The primary side voltage component is transformed into an equivalent secondary voltage component on each phase secondary side of the CMT. This voltage component opposes the VSI CMV, resulting in a significant reduction in the net CMV of EDSs [37]. This will further improves the EDSs performance and reliability. It will also minimizes the risk of electrical interference, equipment malfunction, and damage caused by CMV, ensuring the smoother operation and prolonged lifespan of the drive system components [34, 37].

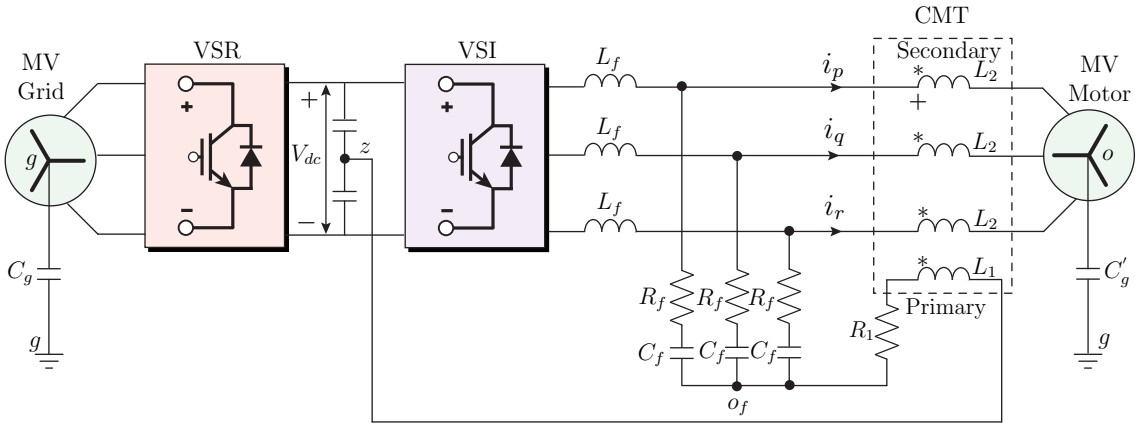


Figure 2.6: MLI-fed EDSs with passive common-mode transformer

However, passive CMT based filters have some disadvantage, such as they are frequency dependent as they are typically designed to target specific frequency ranges and they might not provide sufficient attenuation for all types of CM noise. These filters also introduce power losses into the system which can result in a reduction in EDSs efficiency. They also increases cost, size, and weight of the EDSs [37, 66].

Unlike passive CMT based filters, active CMT-based filters incorporate active electronic components such as power electronic converters as shown in Fig. 2.7 [35]. The power electronic converter acts as an active power filter and produces a voltage component equivalent and opposite phase to the EDSs CMV, at its output terminals. This voltage component will be injected into each phase of the main circuit through a CMT as shown in Fig. 2.7 [35]. The injected voltage component will be in opposite in phase of the load CMV, resulting in a zero CMV at the EDSs [35]. The active CMT-based filters use feedback control mechanisms to continuously monitor and adjust the generated signal to ensure effective cancellation of the CMV [35, 67].

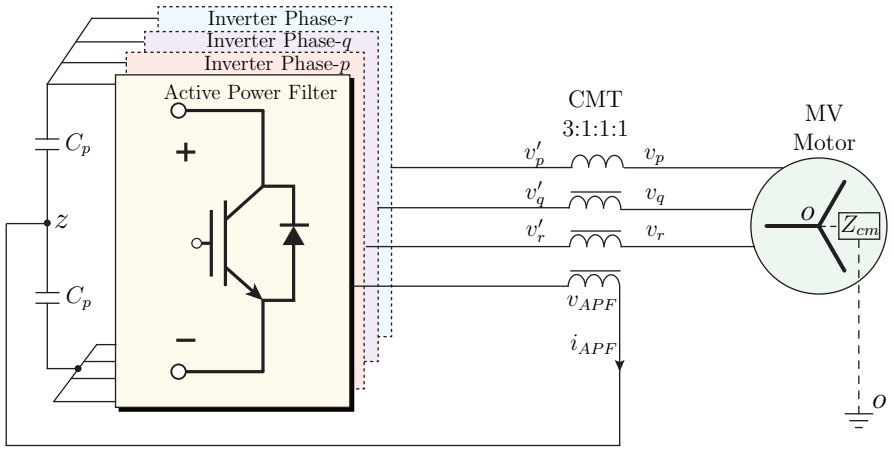


Figure 2.7: MLI-fed EDSs with active common-mode transformer circuit

Even though, the active CMT filters can effectively eliminate the EDSs CMV, they have several drawbacks [35, 68]:

- **Complexity**: Active CMT-based filters are more complex than passive CMT-based filters due to the inclusion of components such as power electronic converters and closed control algorithms, feedback measurement circuits. These circuits increase the design and implementation complexity of the active CMT-based filters.

- **Cost**: The use of power electronic converters and associated control circuitry makes active

CMT-based filters more expensive than passive CMT-based filters. The increased cost will be a serious concern, especially in cost-sensitive application or when deploying the CM filters in large-scale systems.

- **Power Consumption**: The active CMT-based filters require power to operate the power electronic converter components and control circuitry. The power consumption of active CMT-based filters is generally higher than that of passive CMT-based filters, which further affects the EDSs efficiency.

- **Potential and Instability**: The active CMT-based filters rely on feedback control loops to adjust the generated signals and effectively cancel out the CMV. Improper design or implementation of the feedback loops can lead to instability, oscillations, or even system failure.

- **Sensitivity to Noise and Interference**: The active CMT-based filters will be more sensitive to noise and interference compared to passive CMT-based filters, especially in high-frequency or harsh electromagnetic environments. The active components and control circuitry will also introduce noise or susceptibility to external interference, which further degrades the filter performance.

- **Limited Bandwidth**: The active CMT-based filters use a closed-loop controller to adjust their output voltage magnitude in real-time. However, the controllers bandwidth will impact the filter's ability to minimize the CMVs in EDSs.

2.3 Software-Based CMV Minimization Approaches

Hardware-based solutions effectively blocks or minimizes the CMV, but they increases system cost, size, and volume. They also affect the system efficiency due to the power

losses in the additional hardware circuitry. On the other hand, software-based solutions involve modifications and implementation of control algorithms in digital control platforms to mitigate the CMV in MLI-fed EDSs. Some of the software-based solutions are linear control methods with space vector modulation (SVM) schemes [26, 39], sequential model predictive control (SMPC) methods [40, 41], and finite control-set model predictive control (FCS-MPC) methods [27].

2.3.1 Space Vector Modulation Schemes

Space vector modulation (SVM) schemes are widely used with the linear control methods to control the MLIs. It has several key features such as flexibility in selecting the switching vectors to fulfill the control objectives, improved DC-link utilization, improved harmonic performance, and a CMV regulation compared with the carrier-based modulation schemes [69, 70]. The SVM implementation follows the volt-sec balance principle, in which the required space vector is realized by using the nearest three switching vectors in each sampling period. The typical design steps involved in the SVM implementation are depicted in Fig. 2.8, and they are calculation of space vector magnitude and position, sector identification, duty cycles calculation, identifying the nearest switching vectors, and switching sequence formulation [70].

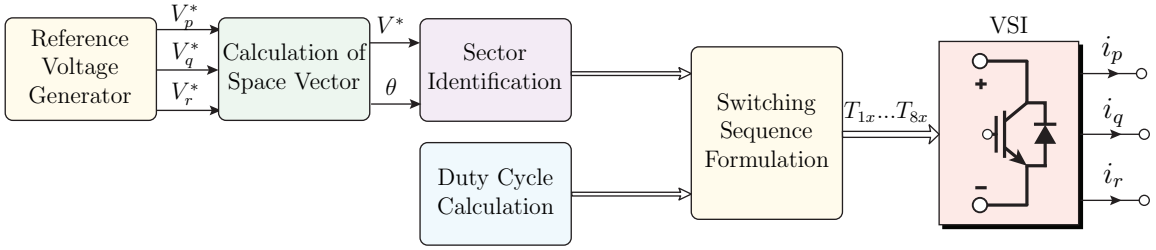


Figure 2.8: Implementation of SVM philosophy.

Among them, the implementation stage of identifying the nearest switching vectors from

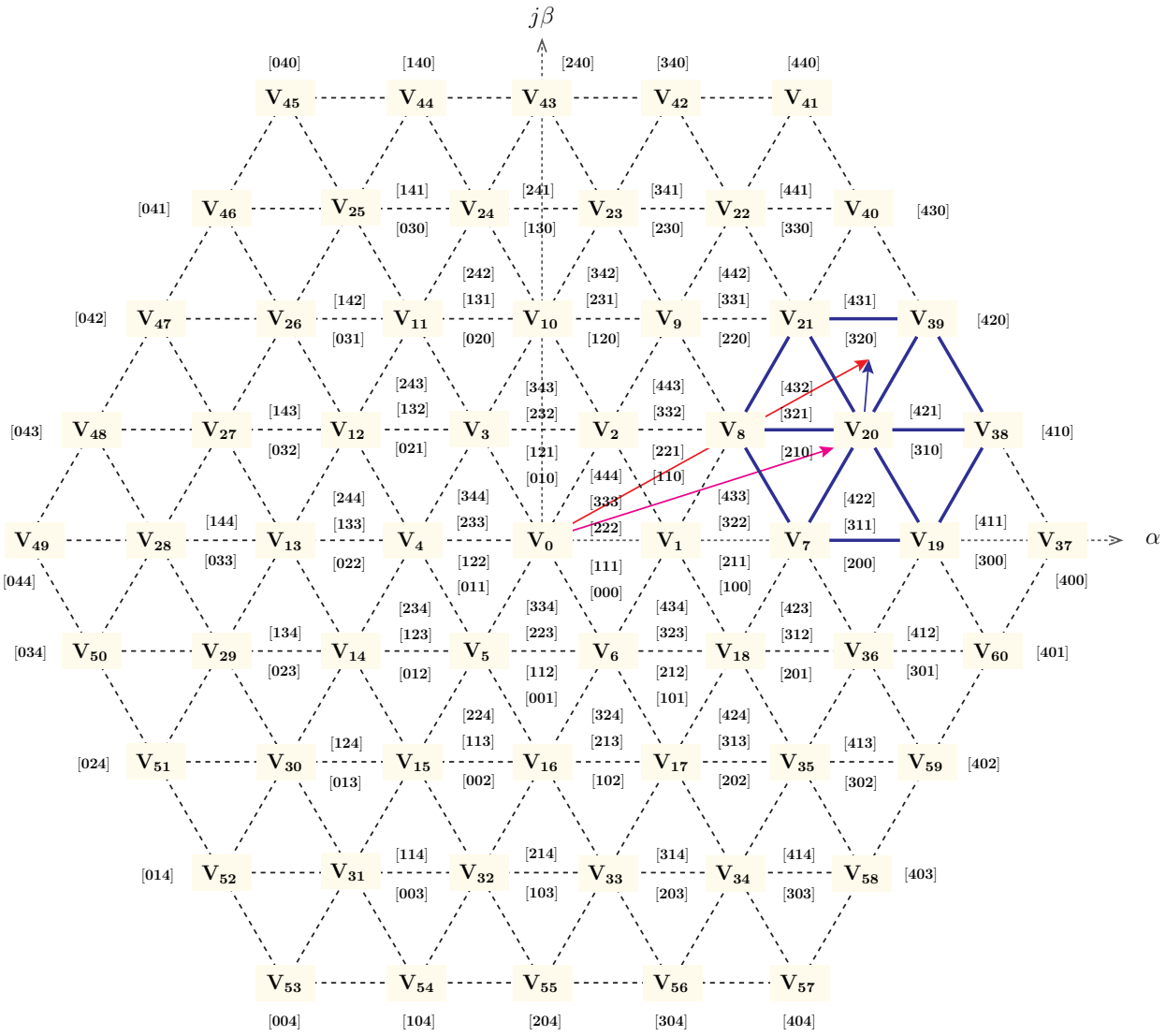


Figure 2.9: Space vector diagram for an FLI.

the available redundancy switching vectors is quite complex. For example, the FLI has a total of 60 switching vectors, which can be realized with a total of 125 switching vector combinations including redundancy switching vectors as shown in Fig. 2.9 [70]. These switching vectors produce different CMV magnitudes at load terminals and selecting the switching vectors with the lowest CMV becomes cumbersome process with the rise in the output levels of MLIs. To identify those vectors in real-time, several SVM implementation philosophies such as $\alpha\beta$, $\alpha\beta\,o$, abc, and gh-references are studied in the literature [26, 42–44, 71, 72]. These

philosophies involve the coordination transformation, which increases the implementation complexity. Other variations in SVM scheme are active zero state PWM (AZSPWM) [73] and near state PWM (NSPWM) [74]. These PWM schemes are designed to use active switching vectors to realize the zero switching vectors, thereby the reducing the CMV magnitude of the inverters.

2.3.2 Sequential Model Predictive Control

The basic principle of sequential model predictive control (SMPC) involves predicting future system behavior over a finite time horizon and optimizing the control actions in a sequential manner to achieve desired objectives while adhering to the system constraints. The SMPC methodology is designed to handle all the control objectives of an MLI in two stages as shown in Fig. 2.10 [50, 75]. These two stages are known as stage-I and stage-II, and they are designed to control the load and inverter objectives. Typically, the three-phase philosophy has been followed in the implementation of stage-I, and it is designed to handle the inverter AC currents and CMV minimization objectives. Traditionally, a cost function is formulated with these two objectives and optimized for all possible switching vectors [40,48]. However, the formulated cost function involves the selection of weighting factors, which affects the control performance of the inverter AC current objective. Alternatively, all possible switching vectors are evaluated in offline by considering the lowest CMV criteria, and eliminated the switching vectors which produce the CMV more than the set limits [41, 49, 76]. However, the offline selection of switching vectors become cumbersome with the rise in output levels of MLIs. Finally, the switching vectors with the lowest CMV only considered in the cost function optimization and identified optimal switching vector [41, 49, 76]. The selected optimal switching vector applied to stage-II.

On the other hand, the per-phase philosophy has been employed in the implementation of

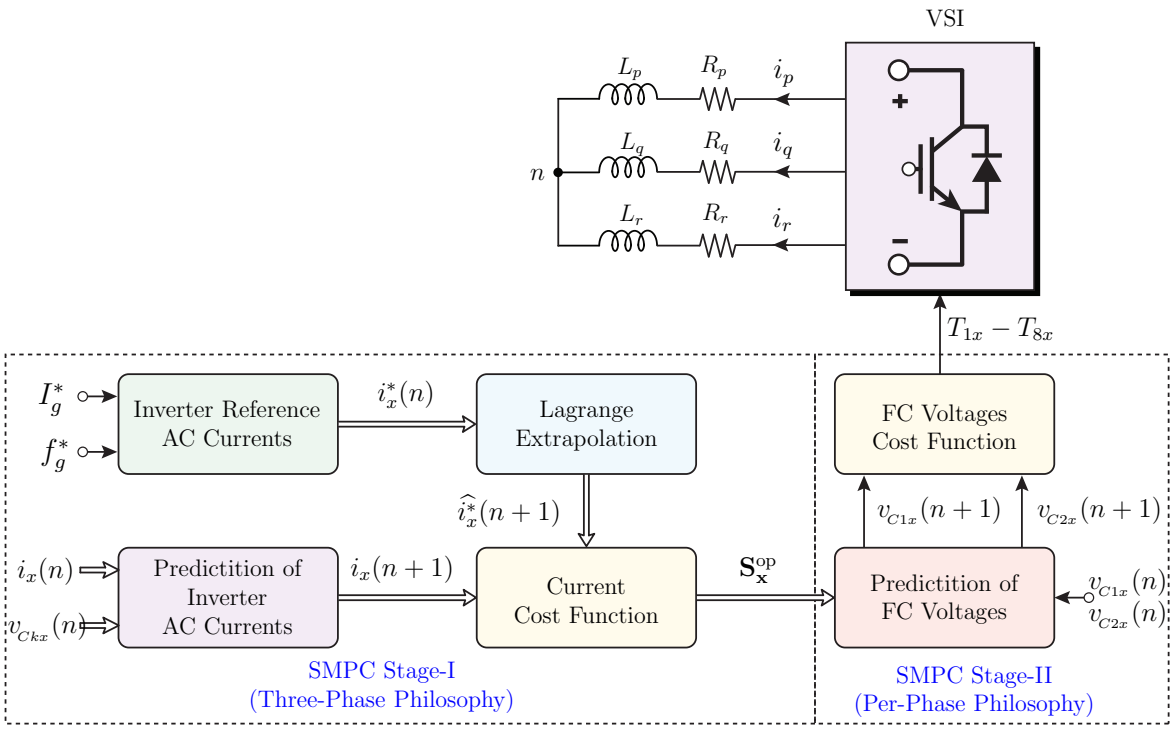


Figure 2.10: Block diagram of SMPC method.

stage-II as shown in Fig. 2.10 [50, 75]. The stage-II is designed to control the FCs voltage of each phase in MLI, independently. A cost function has been formulated with each phase FCs voltage and evaluated for the MLI switching states corresponding to the optimal switching vector only. Finally, the optimal switching state that gives optimal FC voltage is selected and applied to the MLI. Even though, the SMPC effectively fulfills all the control objectives, but it exhibit poor transient response compared to the finite control-set model predictive control (FCS-MPC) methods [50].

2.3.3 Finite Control-Set Model Predictive Control

Finite control-set model predictive control (FCS-MPC) methods have several prominent features such as ease of implementation, intuitive philosophy, fast transient response, ability to handle multiple objectives with a single cost function, easy to compensate control delay,

and flexible to include system constraints and nonlinearities, and attracted a wide range of industrial applications, including MLI-fed EDSs [46, 51, 77]. However, FCS-MPC performance greatly depends on the sampling time, weighting factors, and models accuracy [52].

The design steps involved in the implementation of an FCS-MPC for an MLI is shown in Fig. 2.11 [52]. some of the key design steps are reference generation, extrapolation, prediction, cost function formulation, and optimization. To implement these steps, FCS-MPC requires the MLI mathematical models in discrete-time domain. Typically, the forward Euler method has been employed to derive the discrete-time model from continuous-time models. However, such models have poor accuracy and effects controller tracking performance at large sampling periods [54, 78]. It also leads to high switching frequency operation. To improve the models accuracy, Heun's integration method proposed for MLIs in the literature [55]. However, the use of Heun's integration method-based models increase the real-time computational burden compared to the use of forward Euler's method-based models in FCS-MPC implementation.

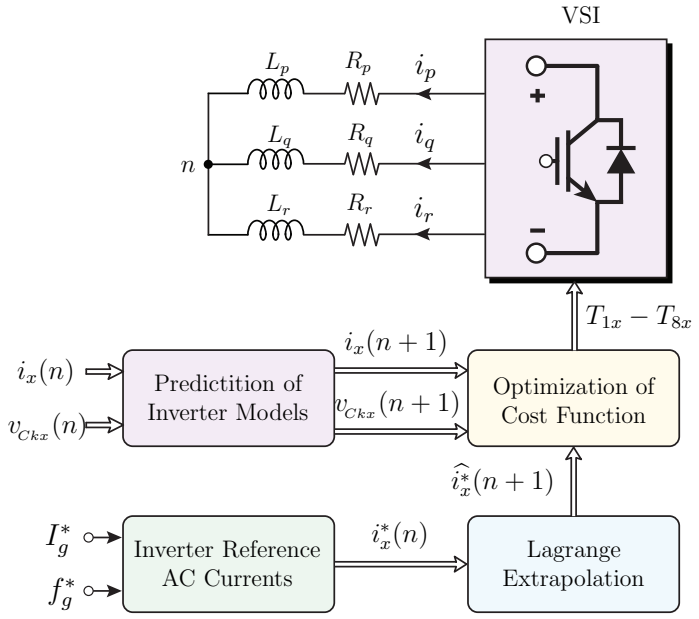


Figure 2.11: Block diagram of FCS-MPC method.

Irrespective of the type of models, FCS-MPC follows a single stage optimization philosophy to achieve all the control objectives in MLIs. In this approach, a single cost function will formulated with all the control objectives (predicted and reference control variables), including inverter AC currents, CMV minimization, and FCS voltage [56, 57]. The cost function is evaluated for all possible switching states of MLI and identified optimal switching state that gives a favourable system response. However, this philosophy requires the proper selection of weighting factors to evaluate the cost value of CMV minimization and FCs voltage objectives against the inverter AC current control objective [79]. The improper selection of weighting factors directly affect the inverter AC current performance including its harmonic distortion and tracking error [58]. Hence, it is necessary to develop FCS-MPC methods without weighting factor dependency to minimize the CMV.

2.4 Summary

In this chapter, hardware-based and software-based solutions for CMV minimization in MLIs have been reviewed. The hardware-based solutions use external hardware circuitry, which leads to an increase in the cost, weight, volume of the system. Also, they affect system efficiency due to the power losses in the hardware components. On the other hand, software-based solutions involve the implementation of control algorithms, and they don't increase the cost and size of the system. Among the available software-based solutions, FCS-MPC is most promising methodology due to its ability to handle multiple control objectives. However, it requires weighting factor dependent cost function to minimize the CMV in MLIs. The improper selection of weighting factor affects the MLI performance. Also, the conventional FSC-MPC methods have a high computational burden.

Chapter 3

A NEW FCS-MPC WITH CMV MINIMIZATION FOR A FIVE-LEVEL INVERTER

3.1 Introduction

The common-mode voltage (CMV) induces bearing currents and shaft voltages in multilevel inverter (MLI) fed electric drive systems (EDSs) and causes bearing failure and shaft breakdown over a long run [20, 21]. To minimize the CMV, software-based solutions are preferred over the hardware-based solutions due to their ability to reduce the volume and cost of the MLI-fed EDSs [26, 27]. Some of the software-based solutions are linear control method with space vector modulation scheme [42, 45], sequential model predictive control (SMPC) methods [40, 80], and finite control-set model predictive control (FCS-MPC) methods [52, 53, 81].

Among them, FCS-MPC has an ability to handle multiple control objectives of MLIs by using a single cost function [82, 83]. It also exhibits superior transient performance compared with the linear control methods and SMPC methods [46, 50]. However, FCS-MPC performance greatly depends on the models accuracy and weighting factors selection [52]. To improve the models accuracy, Heun's integration method has been introduced in place of the forward Euler integration method in the literature for MLIs [54, 84]. However, the use of

Heun's integration method-based models increase the number of computations, resulting in a need of longer execution time for the real-time implementation of FCS-MPC methods for MLIs [55]. Moreover, FCS-MPC methods use weighting factor dependent cost function to minimize the CMV in MLIs [56, 56, 57, 85]. The improper selection of weighting factors directly impact the primary control objective performance such as current harmonic distortion and current tacking error etc.

To address the aforementioned concerns, a new FCS-MPC philosophy is proposed to minimize the CMV in MLIs without using a weighting factor dependent cost function (i.e., indirect approach). The proposed FCS-MPC follows the per-phase implementation philosophy, resulting in an independent control of each phase objectives of MLIs. This philosophy further reduces the execution time of FCS-MPC algorithm in real-time controllers. The proposed FCS-MPC method is applied to a five-level inverter (FLI), and the corresponding discrete-time models are developed by using Heun's integration method. The performance of the proposed FCS-MPC is verified through experimental studies on a dSPACE/DS1103 controlled laboratory prototype. Also, an experimental comparative study of the proposed and conventional FCS-MPC is presented.

The Chapter 3 is organized as follows: the FLI topology and operation are presented in Section 3.2. The continuous-time and discrete-time models of the FLI are also presented in Section 3.2. The implementation of the conventional and the proposed FCS-MPC philosophies are discussed in Sections 3.3 and 3.4, respectively. The experimental performance of the proposed FCS-MPC and its comparison with the conventional FCS-MPC methods are presented in Sections 3.5 and 3.6, respectively.

3.2 Topology and Modeling of FLI

The circuit configuration of an FLI is shown in Fig. 3.1 [78], and it is designed with eight IGBT switching devices with anti-parallel diodes (T_{1x}–T_{8x}), where $x \in \{p, q, r\}$ represents the inverter AC terminal. Among them, T_{1x} and T_{8x} are realized with a series connection of two identical devices of $V_{dc}/4$ blocking voltage each, to handle a net blocking voltage of $V_{dc}/2$, where V_{dc} is the DC-link voltage. On the other hand, T_{2x}–T_{7x} are realized with a single device of $V_{dc}/4$ blocking voltage. In addition, the FLI requires two floating capacitors (FCs) (C_{1x}–C_{2x}) with a rated voltage of $V_{dc}/4$ per phase. The voltage of C_{1x} and C_{2x} are denoted with v_{C1x} and v_{C2x}, respectively, and they are regulated at $V_{dc}/4$ each to achieve a five-level operation by using the device switching states (T_{1x}–T_{8x}) given in Table 3.1 [78]. The AC terminals of FLI is connected to a passive load, which is formed with a series connection of a resistor (R_x) and an inductor (L_x).

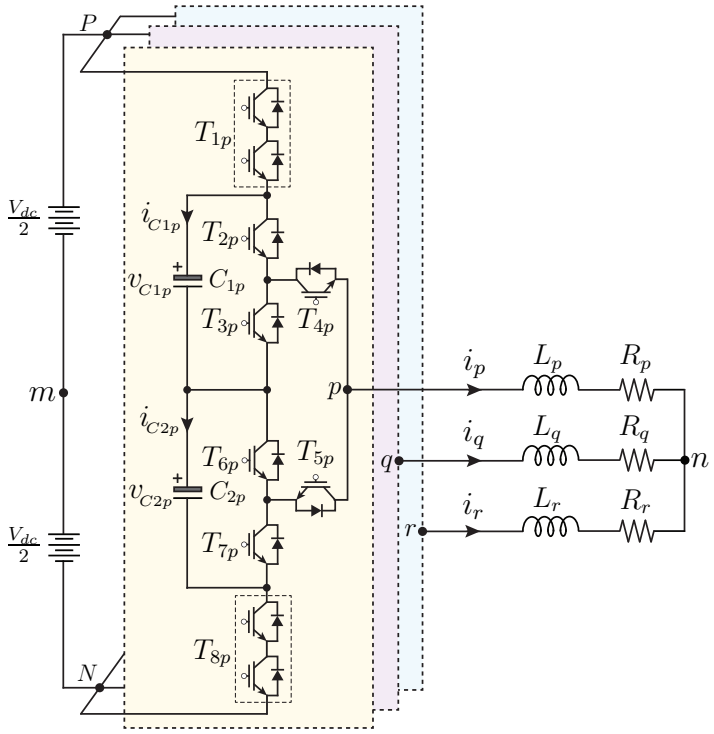


Figure 3.1: Circuit configuration of an FLI.

According to Table 3.1, the FLI has 6 switching states per phase, resulting in a total of 216 (i.e., 6^3) switching combinations to generate a five-level output voltage waveform with a step of $V_{dc}/4$ at the AC terminals of a three-phase FLI. The typical voltage levels of an FLI output voltage (v_{xm}) waveform are $V_{dc}/2$, $V_{dc}/4$, 0, -$V_{dc}/4$, and -$V_{dc}/2$. Depending on the switching state and current direction, the FCs have one of the following states: (i) Charging, (ii) Discharging, and (iii) No Change.

Table 3.1: FLI switching states and their impact on FC voltages

T_{1x}	T_{2x}	T_{3x}	T_{4x}	T_{5x}	T_{6x}	T_{7x}	T_{8x}	v_{C1x}	v_{C2x}	v_{xm}
1	1	0	1	0	0	0	0	No Change	No Change	$\frac{V_{dc}}{2}$
1	0	1	1	0	0	0	0	Charging ($i_x > 0$)	No Change	$\frac{V_{dc}}{4}$
0	1	0	1	0	0	0	1	Discharging ($i_x > 0$)	Discharging ($i_x > 0$)	0
1	0	0	0	1	0	1	0	Charging ($i_x > 0$)	Charging ($i_x > 0$)	0
0	0	0	0	1	1	0	1	No Change	Discharging ($i_x > 0$)	$-\frac{V_{dc}}{4}$
0	0	0	0	1	0	1	1	No Change	No Change	$-\frac{V_{dc}}{2}$

3.2.1 Continuous-time Models of the FLI

The proposed FCS-MPC is designed to control the load currents and FC voltages of FLI. It requires discrete-time mathematical models of the FLI to implement in real-time controllers. The discrete-time models are further derived from continuous-time models and they are given in this subsection. By applying the Kirchhoff's voltage law (KVL) on the FLI AC side shown in Fig. 3.1, the load voltage of phase-x can be written as,

$$v_{xn}(t) = v_{xm}(t) - v_{nm}(t) \tag{3.1}$$

where v_{xn} is load voltage of phase-x, $v_{xm}(t)$ is the FLI AC voltage of phase-x, and $v_{nm}(t)$ is the FLI CMV.

Considering the balanced operation of the FLI (i.e., $i_p(t)+i_q(t)+i_r(t)=0$), the FLI CMV can be written as,

$$v_{nm}(t) = \frac{1}{3} \sum_{x=p,q,r} v_{xm}(t) \tag{3.2}$$

From Fig. 3.1, the FLI AC currents trajectory in the continuous-time domain can be written by applying KVL on the load-side as,

$$\frac{di_x(t)}{dt} = \frac{1}{L_x} v_{xn}(t) - \frac{R_x}{L_x} i_x(t) \tag{3.3}$$

where $i_x(t)$ is the FLI AC current or load current of phase-x.

From (3.1) and (3.3), the FLI AC current trajectory in the continuous-time domain can be rewritten as,

$$\frac{di_x(t)}{dt} = \frac{1}{L_x} \left(v_{xm}(t) - v_{nm}(t)\right) - \frac{R_x}{L_x} i_x(t) \tag{3.4}$$

The FLI has two FCs in each phase, and their voltages should be regulated at $V_{dc}/4$. The trajectory of the k^{th} FC voltage of phase-x can be written as,

$$\frac{dv_{Ckx}}{dt} = \frac{i_{Ckx}}{C_{kx}} \tag{3.5}$$

where v_{Ckx}, i_{Ckx}, and C_{kx} are the (k)th FC's voltage, current, and capacitance of phase-x respectively, and $k \in \{1, 2\}$ is the FC index.

3.2.2 Discrete-Time Models of the FLI

In this study, Heun's integration method is employed to derive the discrete-time models from the continuous-time models. According to the principle of Heun's integration method,

the effective value of the predicted control variable y can be calculated by taking the average of control variables trajectory at the (n)th and the $(n+1)$th sampling points, and it is expressed as [86],

$$y^p(n+1) = \frac{T_s}{2}\left[\frac{d\,y}{dt}\Big|_{t=t(n)} + \frac{d\,y}{dt}\Big|_{t=t(n+1)}\right] + y(n) \tag{3.6}$$

where superscript "p" represents the effective value of the predicted variable, T_s is the sampling time, $dy/dt\big|_{t=t(n)}$ represents the control variable trajectory in the predictor stage, and $dy/dt\big|_{t=t(n+1)}$ represents the control variable trajectory in the corrector stage.

From (3.3) and (3.6), the effective value of the predicted FLI AC currents can be written as,

$$i_x^p(n+1) = \frac{T_s}{2\,L_x}\left(v_{xn}(n) + v_{xn}(n+1)\right) - \frac{T_s\,R_x}{2\,L_x}\left(i_x(n) + i_x(n+1)\right) + i_x(n) \tag{3.7}$$

where $i_x(n)$ is the measured load current. On the other hand, the FLI AC current at the $(n+1)$th sampling point is obtained by discretizing the continuous-time model given in (3.3) by using the forward Euler's integration method, and it is given as,

$$i_x(n+1) = \frac{T_s}{L_x}\,v_{xn}(n) - \frac{T_s\,R_x}{L_x}\,i_x(n) + i_x(n) \tag{3.8}$$

From Table 3.1, the FLI AC voltage of phase-x at the (n)th sampling point is given as,

$$v_{xm}(n) = V_{dc}\,T_{1x} - \frac{V_{dc}}{2} + (T_{2x} - T_{1x})\,v_{C1x}(n) + (T_{8x} - T_{7x})\,v_{C2x}(n) \tag{3.9}$$

where $v_{C1x}(n)$ and $v_{C2x}(n)$ are the measured FC voltages at the (n)th sampling point.

Similarly, the FLI AC voltage of phase-x at the $(n+1)$th sampling point is given as,

$$v_{xm}(n+1) = V_{dc}\, T_{1x} - \frac{V_{dc}}{2} + (T_{2x} - T_{1x})\, v_{C1x}(n+1) + (T_{8x} - T_{7x})\, v_{C2x}(n+1) \tag{3.10}$$

where $v_{C1x}(n+1)$ and $v_{C2x}(n+1)$ are the FC voltage outcomes of predictor stage. These voltages are obtained by discretizing the continuous-time model given in (3.5) by using the forward Euler's integration method, and it is given as,

$$\begin{aligned} v_{C1x}(n+1) &= v_{C1x}(n) + \frac{T_s}{C_{1x}}\, i_{C1x}(n) \\ v_{C2x}(n+1) &= v_{C2x}(n) + \frac{T_s}{C_{2x}}\, i_{C2x}(n) \end{aligned} \tag{3.11}$$

From Table 3.1, the calculation of FCs current at the (n)th sampling point can be written as,

$$\begin{aligned} i_{C1x}(n) &= (T_{1x} - T_{2x})\, i_x(n) \\ i_{C2x}(n) &= (T_{7x} - T_{8x})\, i_x(n) \end{aligned} \tag{3.12}$$

From (3.5) and (3.6), the resultant value of the predicted FLI's FCs voltage can be written as,

$$\begin{aligned} v^p_{C1x}(n+1) &= v_{C1x}(n) + \frac{T_s}{2\,C_{1x}}\,(i_{C1x}(n) + i_{C1x}(n+1)) \\ v^p_{C2x}(n+1) &= v_{C2x}(n) + \frac{T_s}{2\,C_{2x}}\,(i_{C2x}(n) + i_{C2x}(n+1)) \end{aligned} \tag{3.13}$$

From Table 3.1 and equation (3.8), the FCs current at the $(n+1)$th sampling time can be expressed as,

$$\begin{aligned} i_{C1x}(n+1) &= (T_{1x} - T_{2x})\, i_x(n+1) \\ i_{C2x}(n+1) &= (T_{7x} - T_{8x})\, i_x(n+1) \end{aligned} \tag{3.14}$$

3.3 Conventional FCS-MPC Implementation

The conventional FCS-MPC is designed to handle the three-phase FLI objectives such as load currents, FC voltages, and CMV minimization. The implementation steps of the

conventional FCS-MPC is depicted in Fig. 3.2, which follows the three-phase implementation philosophy [55]. In this study, the three-phase FLI reference AC currents are generated with a peak magnitude of I_g^* and a frequency of f_g^*, and they are given as,

$$i_x^*(n) = I_g^* \, cos(2\pi \, f_g^* \, t + \theta_o) \tag{3.15}$$

where θ_o represents the three-phase system phase angle difference.

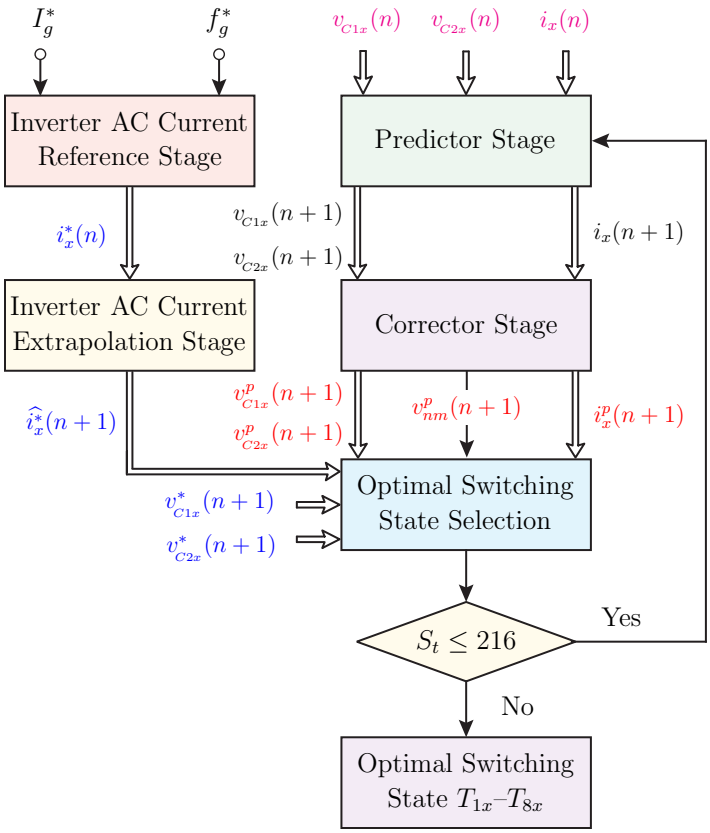


Figure 3.2: Implementation procedure of the conventional FCS-MPC.

The three-phase FLI reference AC currents in (3.15) are time-varying signals, and they are extrapolated to the $(n+1)$th sampling point by using Lagrange extrapolation as follows [55]:

$$\widehat{i}_x^*(n+1) = 3\, i_x^*(n) - 3\, i_x^*(n-1) + i_x^*(n-2) \tag{3.16}$$

In this study, the reference value of FCs voltage at the (n)th sampling point is defined, and it is set to $v^*_{C1x}(n) = v^*_{C2x}(n) = V_{dc}/4$. These signals are DC in nature, and they remain constant at all sampling points. Hence, the $v^*_{C1x}(n+1) = v^*_{C1x}(n)$ and $v^*_{C2x}(n+1) = v^*_{C2x}(n)$. On the other hand, the prediction process of control variables involves the calculation of trajectories at predictor and corrector stages as shown in Fig. 3.2. Initially, the three phase load currents ($i_x(n)$) and FC voltages ($v_{C1x}(n)$ and $v_{C2x}(n)$) are measured at the (n)th sampling point. These measured values are used in the predictor stage to calculate the three-phase load currents and FC voltages at the $(n+1)$th sampling point by using the equations (3.8), (3.9), (3.11), and (3.12). The measured control variables ($i_x(n)$, $v_{C1x}(n)$, and $v_{C2x}(n)$) together with the predictor stage outcomes ($i_x(n+1)$, $v_{C1x}(n+1)$, and $v_{C2x}(n+1)$) are used in the corrector stage to calculate the resultant value of the predicted control variables ($i^p_x(n+1)$, $v^p_{C1x}(n+1)$, and $v^p_{C2x}(n+1)$) by using equations (3.7), (3.10), (3.13), and (3.14). On the other hand, the CMV directly depends on the inverter AC voltage and its predicted value at the $(n+1)$th sampling point can be obtained from equation (3.2) and (3.10) as,

$$v^p_{nm}(n+1) = \frac{1}{3}\sum_{x=p,q,r} v_{xm}(n+1) \tag{3.17}$$

Finally, a single cost function is formulated with the predicted and reference control variables of three-phases together, and it is given as,

$$\begin{aligned} J(n) = &\sum_{x=p,q,r} [\widehat{i^*_x}(n+1) - i^p_x(n+1)]^2 + \lambda_v \sum_{x=p,q,r} [v^*_{C1x}(n+1) - v^p_{C1x}(n+1)]^2 \\ &+ \lambda_v \sum_{x=p,q,r} [v^*_{C2x}(n+1) - v^p_{C2x}(n+1)]^2 + \lambda_m \left[v^*_{nm}(n+1) - v^p_{nm}(n+1)\right]^2 \end{aligned} \tag{3.18}$$

where λ_v and λ_m are the weighting factors of the FCs voltage and the CMV objectives, respectively, and they are selected as per-unit method given in [47, 56]. The cost function $J(n)$ is evaluated for a total of 216 switching states (S_t). Finally, the switching state with

the lowest cost value is selected and applied to the FLI. However, the FLI AC currents (i.e., load voltage component) and CMV are the function of inverter AC output voltage, resulting in a coupling between these two objectives as per equation (3.2) and (3.4). Hence, the minimization of CMV with the help of a cost function affects the FLI AC current control performance, which leads to increase in the current harmonic distortion. Furthermore, the conventional FCS-MPC needs longer execution time to implement in real-time controllers due to the presence of 216 predictions.

3.4 Proposed FCS-MPC Implementation

In the conventional FCS-MPC method, the cost function has been employed to minimize the CMV ($v_{nm}(t)$) and its magnitude depends on the reference value of the CMV ($v^*_{nm}(t)$). On the contrary, in the proposed FCS-MPC method, the objective of $v_{nm}(t)$ minimization is integrated into the FLI's AC current control objective by assuming that $v^*_{nm}(t) = v_{nm}(t) \approx 0$ at steady-state. Considering this assumption, from (3.1) and (3.4), the simplified FLI's AC currents trajectory with an integrated CMV minimization objective can be expressed as,

$$\frac{di_x(t)}{dt} = \frac{1}{L_x}\, v_{xm}(t) - \frac{R_x}{L_x}\, i_x(t) \tag{3.19}$$

Typically, the FLI AC voltage ($v_{xm}(t)$) consists of load voltage ($v_{xn}(t)$) and CMV ($v_{nm}(t)$) components. The load voltage component magnitude will be regulated by controlling the FLI AC currents or load currents, whereas the CMV limits are set by the user. According to (3.19), by controlling the inverter ac currents, the FLI produces an AC voltage equal to the load voltage component (i.e., $v_{xm}(t) = v_{xn}(t)$), which indirectly implies that the FLI AC voltage will have a CMV component close to zero (i.e., the lowest magnitude).

By applying Heun's integration method, the continuous-time model in (3.19) is converted

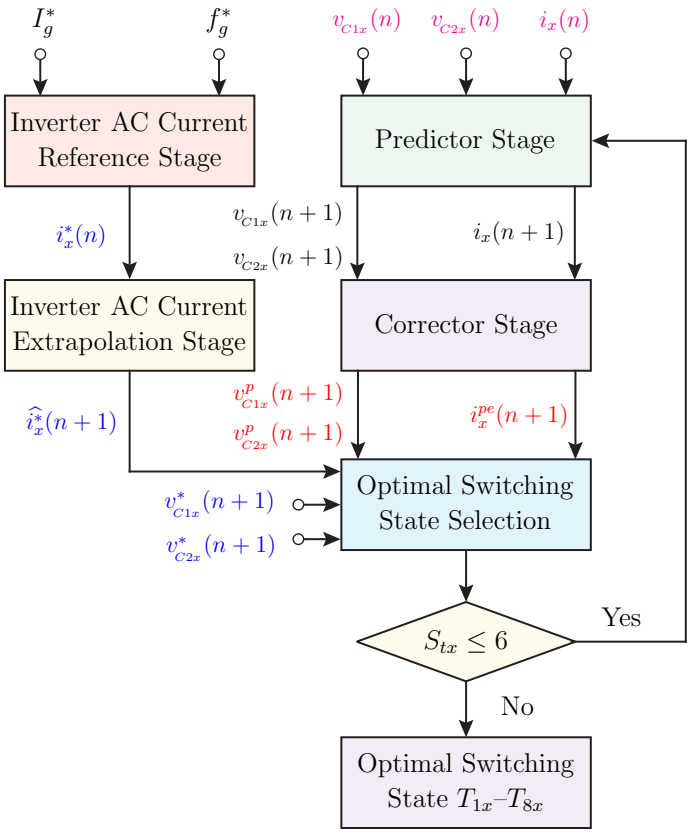


Figure 3.3: Implementation procedure of the proposed FCS-MPC.

into discrete-time domain, and the resultant predicted FLI AC current is given as,

$$i_x^{pe}(n+1) = \frac{T_s}{2\,L_x}\left(v_{xm}(n) + v_{xm}(n+1)\right) - \frac{T_s\,R_x}{2\,L_x}\left(i_x(n) + i_x(n+1)\right) + i_x(n) \tag{3.20}$$

whereas the predictive models of FC voltages are remain the same as given in (3.13).

The FLI inverter AC voltages at the (n)th and $(n+1)$th sampling points are calculated by using (3.9) and (3.10), respectively. According to (3.20), the control of phase-x current directly depends on their respective phase voltages (i.e., switching states and FC voltages) only, resulting in an independent control of each phase objectives with the proposed FCS-MPC. This further results in the per-phase implementation philosophy of the proposed FCS-MPC, and the corresponding design steps are shown in Fig. 3.3. In this method, the FLI

reference AC currents are generated with a peak value of I_g^* and f_g^* and they are defined in (3.15). These currents are extrapolated to the $(n+1)$th sampling point by using Lagrange extrapolation technique, and the extrapolated reference AC currents are given in (3.16).

On the other hand, the prediction process of control variables involves the predictor and corrector stages in the implementation of the proposed FCS-MPC approach. In this method, each phase load current ($i_x(n)$) and FC voltages ($v_{C1x}(n)$ and $v_{C2x}(n)$) are measured at the (n)th sampling point. These measured values are used in the predictor stage to calculate the corresponding phase-x load currents and FC voltages at the $(n+1)$th sampling point by using the equations (3.8), (3.9), (3.11), and (3.12). The measured control variables of phase-x ($i_x(n)$, $v_{C1x}(n)$, and $v_{C2x}(n)$) together with the predictor stage outcomes ($i_x(n+1)$, $v_{C1x}(n+1)$, and $v_{C2x}(n+1)$) are used in the corrector stage to calculate the resultant value of the predicted control variables of phase-x ($i_x^{pe}(n+1)$, $v_{C1x}^{p}(n+1)$, and $v_{C2x}^{p}(n+1)$) by using equations (3.20), (3.10), (3.13), and (3.14).

Finally, the cost function ($J_x(n)$) for each phase is formulated with their respective phase objectives (i.e., the predicted and reference control variables of phase-x), and it is given as,

$$\begin{aligned} J_x(n) = {} & [\widehat{i_x^*}(n+1) - i_x^{pe}(n+1)]^2 + \lambda_v \left[v_{C1x}^*(n+1) - v_{C1x}^{p}(n+1)\right]^2 \\ & + \lambda_v [v_{C2x}^*(n+1) - v_{C2x}^{p}(n+1)]^2 \end{aligned} \tag{3.21}$$

where λ_v is the weighting factor of the FCs voltage objective, and it is selected as per-unit method given in [47,56]. The cost function of each phase ($J_x(n)$) is evaluated for a total of 6 switching states (S_{tx}). Finally, the switching state that gives a favourable system response is selected and applied to the FLI. The selected switching state ensures the FLI AC currents and FC voltages follow their respective references, while producing the lowest CMV. Moreover, the proposed FCS-MPC involves a total 18 (=3×6) predictions in a sampling time, which are significantly less than the conventional FCS-MPC. Hence, the proposed FCS-MPC needs a

shorter execution time, and it is highly feasible to implement in real-time control platforms.

3.5 Experimental Study

The experimental studies are conducted on a 6.5 kVA rated FLI laboratory prototype as shown in Fig. 3.4. The system specifications of the laboratory prototype are given in Table 3.2. The FLI is constructed with Semikron SKM100GB12T4 devices, SKHI22B gate drivers, and EPCOS DC capacitors.

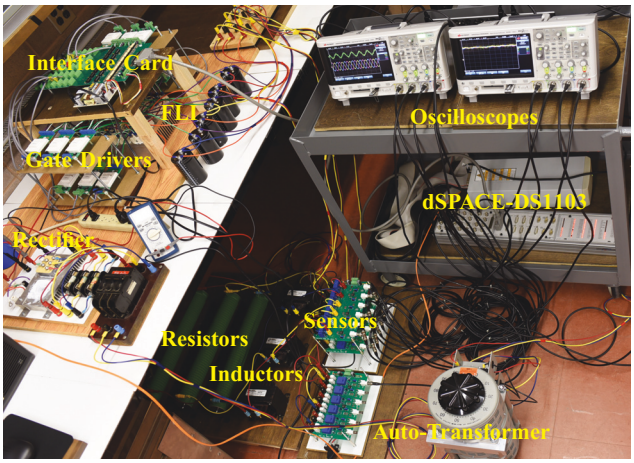


Figure 3.4: Laboratory prototype of an FLI.

The DC-link of an FLI is rated to 280 V, and it is generated by using an auto-transformer and a diode-bridge rectifier as shown in Fig 3.4. For five-level operation, each FC is designed with a capacitance of 2200 μF and a rated voltage of 70 V. The AC terminals of an FLI are connected to a three-phase passive load, which is formed with a series connection of a 5 Ω resistance and a 5 mH inductance. The proposed FCS-MPC algorithm is implemented in the dSPACE/DS1103 rapid control platform, and it is executed with a sampling time (T_s) of 200 μs, The performance of the proposed FCS-MPC method is evaluated in terms of total demand distortion of the FLI AC currents (%TDD$_i$), root mean square (RMS) value of the CMV (V_{cm}), average switching frequency (f_{sw}), and computational burden. Additionally,

Table 3.2: Laboratory prototype specifications

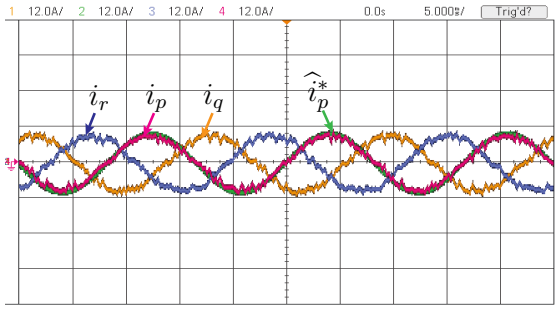
Parameters Description	Value
Inverter rated power (S_{gr})	6.5 kVA
Inverter rated voltage (V_{gr})	208 V (L-L)
Inverter rated current (I_{gr})	17.68 A (rms)
Inverter rated frequency (f_{gr})	60 Hz
DC-link voltage V_{dc}	280 V
FC voltage (V_{Ckx})	70 V
FC capacitance (C_{kx})	2200 μF
Load inductance (L_x)	5 mH
Load resistance (R_x)	5 Ω
Sampling time (T_s)	200 μs

the proposed FCS-MPC performance is compared with the existing FCS-MPC methods [55] with and without CMV minimization.

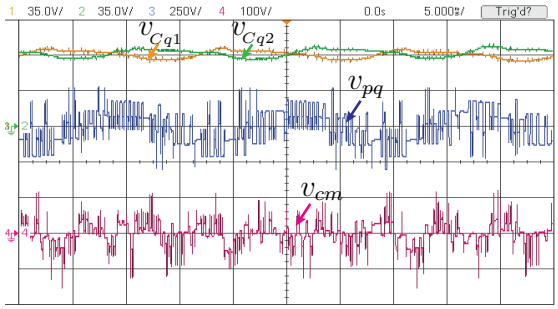
3.5.1 Steady State Performance of the Proposed FCS-MPC

The steady-state performance of the proposed FCS-MPC with the reference current magnitude (I_g^*) of 10 A and the reference frequency (f_g^*) of 60 Hz is shown in Fig. 3.5. The results show that the FLI AC currents follow their respective reference currents as shown in Fig. 3.5(a), and they have a %TDD$_i$ of 1.94. Each FC voltage is perfectly regulated at 70 V as shown in Fig. 3.5(b). The FLI produces a line-to-line voltage with 5 steps. It has a voltage total harmonic distortion (%THD$_v$) of 80.62 while operating at a switching frequency (f_{sw}) of 725 Hz. Also, the V_{cm} of FLI is around 28.86 V at $I_g^* = 10$ A.

Similar, the steady-state performance of the proposed FCS-MPC at $I_g^* = 25$ A and $f_g^* = 60$ Hz is presented in Fig. 3.6. Under this scenario, the proposed FCS-MPC produces a %TDD$_i$ and %THD$_v$ of 2.06 and 29.09 as shown in Figs. 3.6(a) and 3.6(b), respectively. Each FC

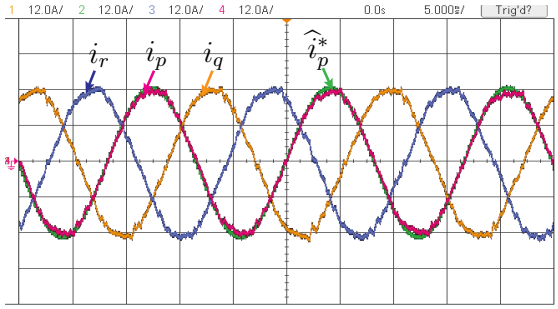


(a) Three-phase load currents

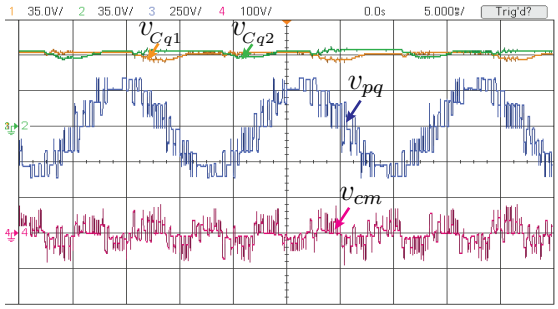


(b) FC voltages, Load voltage, and CMV

Figure 3.5: Steady-state performance at $I_g^* = 10$ A and $f_g^* = 60$ Hz.



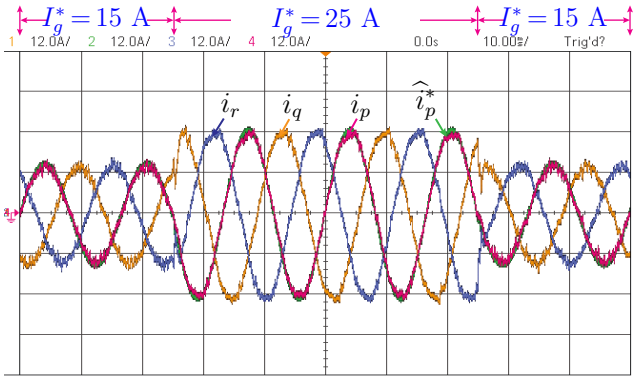
(a) Three-phase load currents



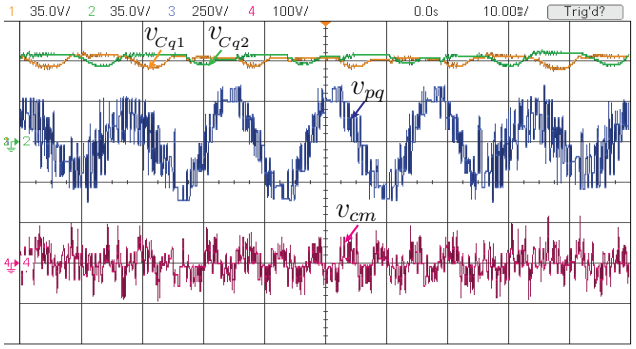
(b) FC voltages, Load voltage, and CMV

Figure 3.6: Steady-state performance at $I_g^* = 25$ A and $f_g^* = 60$ Hz.

voltage is regulated at its nominal value of 70 V. Also, the f_{sw} of FLI is around to 525 Hz, which is less than the f_{sw} at 10 A operation. The V_{cm} of FLI is around 24.56 V at $I_g^* = 25$ A.



(a) Three-phase load currents



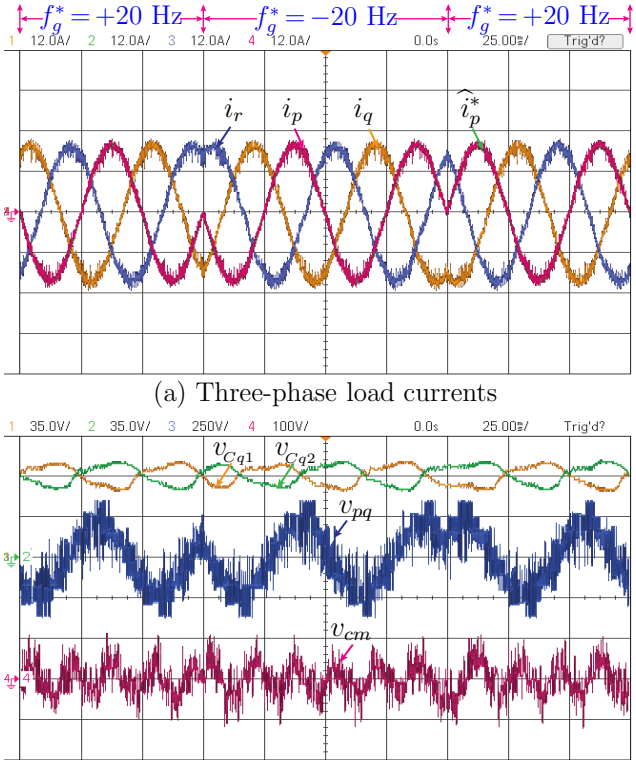
(b) FC voltages, Load voltage, and CMV

Figure 3.7: Dynamic performance with a step change in current magnitude at $f_g^* = 60$ Hz.

3.5.2 Dynamic Performance of Proposed FCS-MPC

The test results of the proposed FCS-MPC with the step change in I_g^* from 15 A to 25 A and from 25 A to 15 A at $f_g^* = 60$ Hz are depicted in Fig. 3.7. The actual FLI AC currents track well their respective references, irrespective of the I_g^* as shown in Fig. 3.7(a). These currents have a %TDD$_i$ of 2.12 at $I_g^* = 15$ A, and it is reduced to 2.06 at $I_g^* = 25$ A. Following Ohm's law, the FLI AC voltage magnitude increases with the rise in I_g^* as shown in Fig. 3.7(b). The FLI AC voltage has a %THD$_v$ of 76.2 at $I_g^* = 15$ A and 29.09 at

$I_g^* = 25$ A. The FCs voltage is perfectly regulated at 70 V each, irrespective of I_g^* as depicted in Fig. 3.7(b). With the proposed FCS-MPC, the FLI produces a CMV of 24.92 V at $I_g^* = 15$ A and 24.56 V at $I_g^* = 25$ A.



(a) Three-phase load currents

(b) FC voltages, Load voltage, and CMV

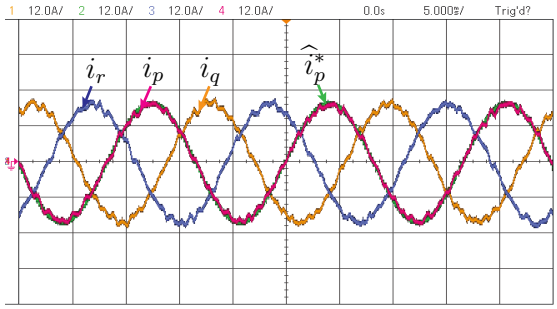
Figure 3.8: Dynamic performance with frequency reversal operation at $I_g^* = 20$ A.

Similarly, the test results of the proposed FCS-MPC with the reversal of f_g^* from +20 Hz to −20 Hz and from −20 Hz to +20 Hz at $I_g^* = 20$ A are depicted in Fig. 3.8. Irrespective of the f_g^*, the reference and actual FLI AC currents closely follow each other as depicted in Fig. 3.8(a), and they have a %TDD$_i$ of 2.53. The FLI produces a voltage waveform equivalent to a five-level operation as shown in Fig. 3.8(b), and it has a %THD$_v$ of 53.58. During this process, the phase-q FCs voltage is perfectly regulated at an average voltage of 70 V each, as depicted in Fig. 3.8(b), while producing a CMV of 33.08 V. Overall, the test results are testimony to the proposed FCS-MPC method's superiority in regulating the FLI

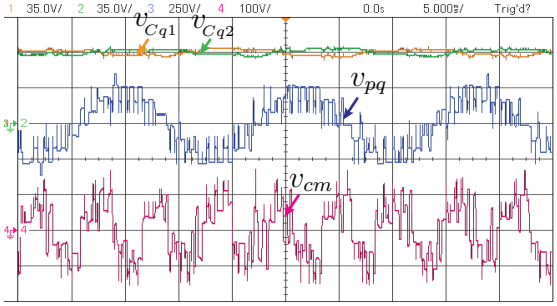
AC currents and FCs voltage objectives of each phase, while minimizing the CMV without using a cost function.

3.6 Experimental Comparison Analysis

The superiority of the proposed FCS-MPC is further demonstrated through a comprehensive comparison with the conventional FCS-MPC methods without and with CMV minimization [55]. The performance comparison is conducted experimentally on a dSPACE controlled FLI laboratory prototype. The reference voltage of each FC is set to 70 V and the FCS-MPC algorithm is executed with a T_s of 200 μs. Figs. 3.9, 3.10, and 3.11 show the experimental performance of the conventional FCS-MPC without CMV minimization, the conventional FCS-MPC with CMV minimization, and the proposed FCS-MPC, respectively at $I_g^* = 20$ A and $f_g^* = 60$ Hz.

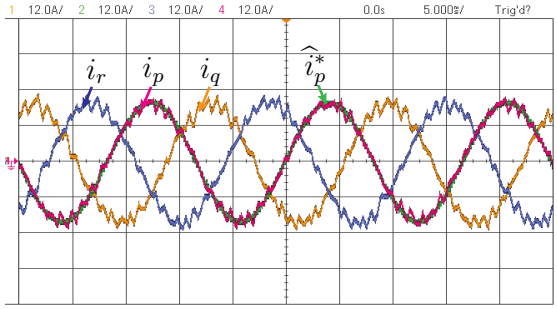


(a) Three-phase load currents

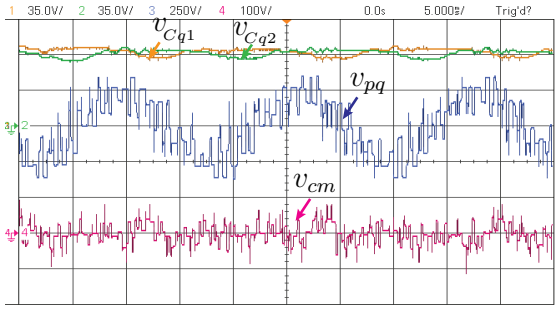


(b) FC voltages, Load voltage, and CMV

Figure 3.9: Experimental performance of the conventional FCS-MPC without CMV minimization at $I_g^* = 20$ A and $f_g^* = 60$ Hz.



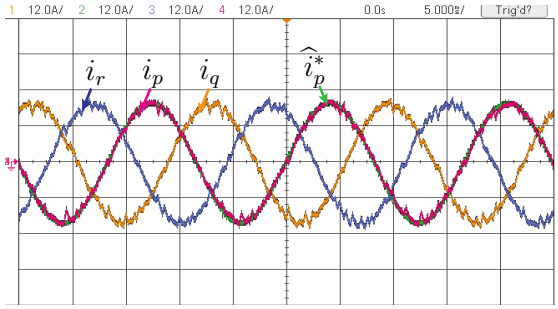
(a) Three-phase load currents



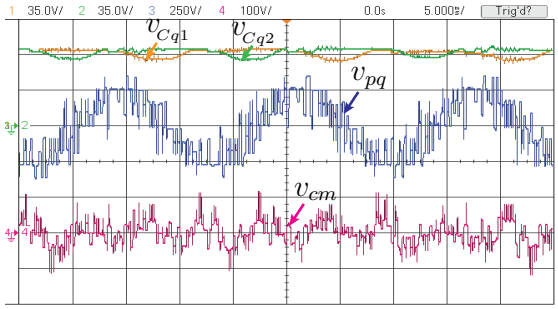
(b) FC voltages, Load voltage, and CMV

Figure 3.10: Experimental performance of the conventional FCS-MPC with CMV minimization at $I_g^* = 20$ A and $f_g^* = 60$ Hz.

Irrespective of the methodology, the FLI produces three-phase load currents corresponding to their reference commands as depicted in Figs. 3.9(a), 3.10(a), and 3.11(a). However, the conventional FCS-MPC without and with CMV minimization produces a $\%\text{TDD}_i$ of 2.16 and 3.19, respectively, whereas the proposed FCS-MPC produces a $\%\text{TDD}_i$ of 2.14. Also, all the FCS-MPC methods perfectly maintains each FC voltage at its nominal value of 70 V as depicted in Figs. 3.9(b), 3.10(b), and 3.11(b). The FLI has a $\%\text{THD}_v$ of 30.18 and 54.82 with the conventional FCS-MPC without and with CMV minimization methods, respectively, whereas the proposed FCS-MPC method produces a $\%\text{THD}_v$ of 45.93 at $I_g^* = 20$ A and $f_g^* = 60$ Hz. Furthermore, the FLI operates at an f_{sw} of 487 Hz and 473 Hz with the conventional FCS-MPC methods without and with CMV minimization, respectively. On the other hand, the proposed FCS-MPC operates at an f_{sw} of 662 Hz at $I_g^* = 20$ A and $f_g^* = 60$ Hz. The FLI produces a V_{cm} of 68.95 V with the conventional FCS-MPC without



(a) Three-phase load currents



(b) FC voltages, Load voltage, and CMV

Figure 3.11: Experimental performance of the proposed FCS-MPC at $I_g^* = 20$ A and $f_g^* = 60$ Hz.

CMV minimization, and it is reduced to 29.63 V and 29.08 V with the conventional FCS-MPC with CMV minimization and the proposed FCS-MPC. Overall, these results proves that the proposed FCS-MPC effectively minimizes the CMV without using any cost function while producing the lowest $\%\text{TDD}_i$. However, the proposed FCS-MPC operates at higher switching frequency compared to the conventional methods.

3.6.1 CMV Minimization

The CMV minimization ability of the proposed FCS-MPC is compared with the conventional FCS-MPC (without and with CMV minimization) at different operating points and the corresponding results are shown in Fig. 3.12(a). The results show that the FLI produces the highest CMV under normal scenarios (without CMV minimization), but it is significantly minimized with the conventional FCS-MPC (with CMV minimization) and the

proposed FCS-MPC. However, at lower value of I_g^*, the proposed FCS-MPC out-performs the conventional FCS-MPC due to the elimination of weighting factor dependent cost function. On the other hand, at high value of I_g^*, both the methods have shown similar performance in minimization of CMV.

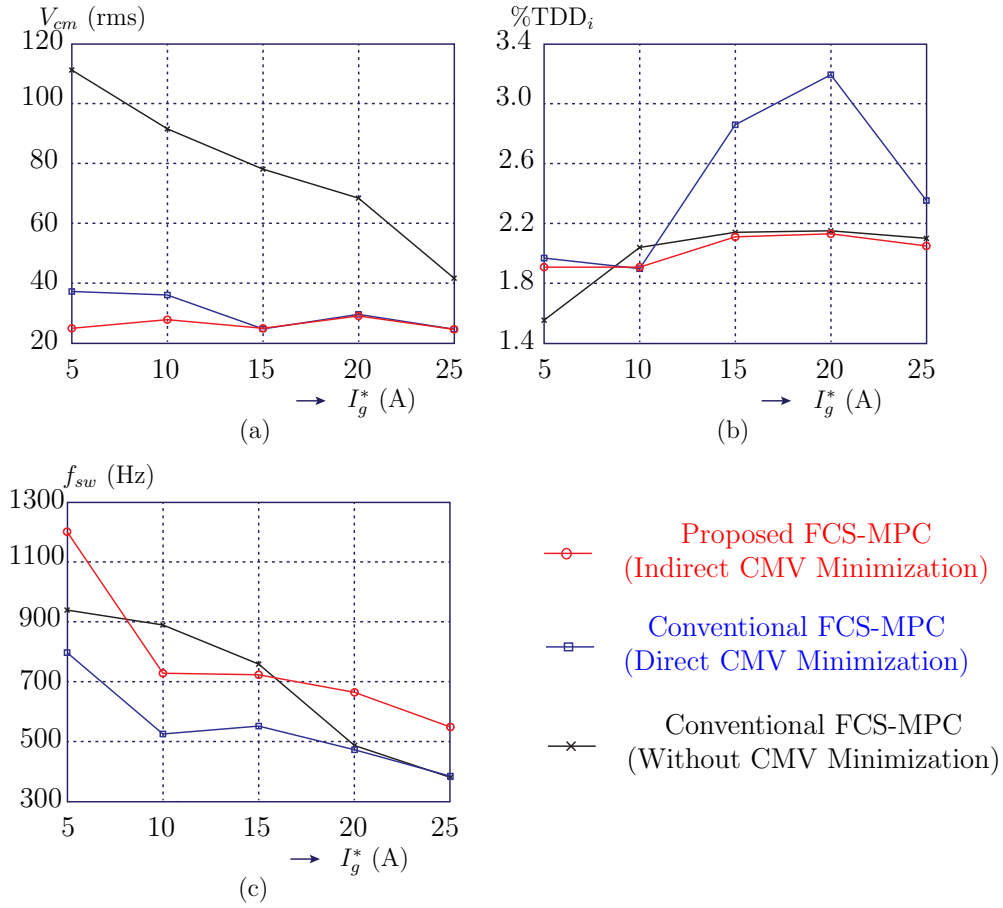


Figure 3.12: Experimental performance comparison: (a) Common-mode voltage (V_{cm}), (b) Total demand distortion (%TDD$_i$), and (c) Average switching frequency (f_{sw}).

3.6.2 Harmonic Performance

The performance of the proposed FCS-MPC is further compared with the conventional FCS-MPC (without and with CMV minimization) methods in terms of %TDD$_i$ at different values of I_g^*, and the corresponding results are depicted in Fig. 3.12(b). The results show that

the %TDD$_i$ increases with the rise in I_g^* value, irrespective of the methodology. Furthermore, the proposed FCS-MPC produces the lowest %TDD$_i$ compared with the conventional FCS-MPC (without and with CMV minimization). Overall, the proposed FCS-MPC produces the lowest %TDD$_i$ while effectively minimizing the CMV compared with the conventional methods.

3.6.3 Average Switching Frequency

Fig. 3.12(c) portrays the f_{sw} comparison of the proposed FCS-MPC with the conventional FCS-MPC (without and with CMV minimization) methods. Irrespective of the methodology, the f_{sw} decreases with the rise in I_g^* value. Furthermore, the proposed FCS-MPC causes high switching frequency operation compared with the conventional FCS-MPC methods with CMV minimization. It further leads to rise in switching losses of the FLI, which is one of drawbacks of the proposed FCS-MPC.

Table 3.3: Computational burden comparison

MPC Method	Maximum Number of Predictions	Minimum Execution Time
Existing FCS-MPC [55]	$6^3 = 216$	115 μs
Proposed FCS-MPC	$3 \times 6 = 18$	14 μs

3.6.4 Computational Burden

In the experimental studies, the dSPACE-DS1103 control platform is utilized to implement both the conventional and the proposed FCS-MPC algorithms. They need a minimum sampling time referred to as a computational burden, to execute all tasks, including the sampling and conversion process of analog-to-digital signals, predictive algorithm execution, and gating signal generation without task overrun error in the dSPACE control platform.

Table 3.3 shows the comparison of the computational burden between the conventional and the proposed FCS-MPC methods. It shows the conventional FCS-MPC method involves a total of 216 predictions, and they need a minimum sampling time of 115 μs to complete all tasks. On the other hand, the proposed FCS-MPC involves only 6 predictions per phase and a total of 18 predictions in a three-phase FLI as given in Table 3.3. Hence, it takes a minimum sampling time of 14 μs to complete all tasks in dSPACE-DS1103 without task overrun error. These results prove that the proposed FCS-MPC's computational burden is relatively low, which is 87.83% less in comparison to the conventional FCS-MPC methods.

Chapter 4

CONCLUSION AND FUTURE WORK

4.1 Conclusion

In this thesis, an FCS-MPC method with indirect CMV minimization capability is proposed for an FLI. The proposed FCS-MPC is formulated by using the per-phase philosophy and it is highly effective in handling each phase control objectives of an FLI, independently. Furthermore, for the real-time implementation of the proposed FCS-MPC, Heun's integration method is adopted in developing the discrete-time models of an FLI. During the development of mathematical models, the objective of CMV minimization is integrated into the FLI AC current models itself. Therefore, the weighting factor dependent cost function and offline selection of switching vectors to reduce CMV is not required. The proposed FCS-MPC method's superiority is demonstrated on a dSPACE-DS1103 controlled laboratory prototype. The test results confirm that the FLI AC currents and FCs voltages are perfectly regulated as per their reference commands. Also, a comparative study of the conventional and the proposed FCS-MPC methods is presented, and the corresponding results are summarized in Table 4.1. The results prove that the proposed FCS-MPC produces the lowest CMV without using a cost function and had shown an excellent controllability of the FCs voltage, along with a low TDD in the FLI AC currents. In addition, the computational burden of the

proposed FCS-MPC is 87.83% lesser in comparison to the existing FCS-MPC methodologies. However, the proposed FCS-MPC causes high switching frequency operation of FLI, which further leads to a higher switching losses compared with the conventional FCS-MPC methods.

Table 4.1: Comparison summary of FCS-MPC methods

Characteristics	Conventional FCS-MPC [55]	Proposed FCS-MPC
Implementation Philosophy	Three-Phase	Per-Phase
Discretization Method	Heun's	Heun's
Cost Function for CMV Minimization	Required	Not Required
CMV Magnitude	Low	Low
Computational Burden	High (115 μs)	Low (14 μs)
Current TDD	High	Low
Switching Frequency	Low	High

4.2 Future Work

There are some challenging issues in the proposed FCS-MPC, which will be considered for future investigation. Some of the issues are:

1) The high switching frequency operation of the proposed FCS-MPC is not desirable for high-power MLIs, as it increases the switching losses. Hence, developing an MPC method with the low switching frequency is an interesting future work.

2) Even though, the proposed FCS-MPC does not require weighting factor selection to minimize the CMV, still it requires weight factor selection for FCs voltage control. Hence,

developing an MPC method with the complete elimination of weighting factors is another interesting work.

3) While addressing the above concerns, it is necessary to keep the current harmonic distortion and computational burden at the lowest value.

Bibliography

[1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug 2010.

[2] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. . M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, Nov 2009.

[3] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A review," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 135–151, Jan 2016.

[4] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun 2008.

[5] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug 2002.

[6] J. Rodriguez, S. Bernet, B. Wu, J. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec 2007.

[7] B. Wu and M. Narimani, *High-power converters and AC drives*, 2nd ed. Wiley-IEEE Press, Jan 2017.

[8] V. Yaramasu, B. Wu, P. C. Sen, S. Kouro, and M. Narimani, "High-power wind energy conversion systems: State-of-the-art and emerging technologies," *Proc. IEEE*, vol. 103, no. 5, pp. 740–788, May 2015.

[9] F. Blaabjerg, Y. Yang, K. A. Kim, and J. Rodriguez, "Power electronics technology for large-scale renewable energy generation," *Proc. IEEE.*, vol. 111, no. 4, pp. 335–355, Apr 2023.

[10] R. Marquardt, "Modular multilevel converters: State of the art and future progress," vol. 5, no. 4, pp. 24–31, Dec 2018.

[11] H. J. Knaak, "Modular multilevel converters and hvdc/facts: A success story," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, Aug 2011, pp. 1–6.

[12] X. Yu, Y. Wei, and Q. Jiang, "Statcom operation scheme of the cdsm-mmc during a pole-to-pole dc fault," *IEEE Trans. Power Del.*, vol. 31, no. 3, pp. 1150–1159, June 2016.

[13] F. Ma, Q. Xu, Z. He, C. Tu, Z. Shuai, A. Luo, and Y. Li, "A railway traction power conditioner using modular multilevel converter and its control strategy for high-speed railway system," *IEEE Trans. Transport. Electrific.*, vol. 2, no. 1, pp. 96–109, Mar 2016.

[14] A. Poorfakhraei, M. Narimani, and A. Emadi, "A review of multilevel inverter topologies in electric vehicles: Current status and future trends," *IEEE Open J. Power Electron.*, vol. 2, pp. 155–170, 2021.

[15] D. Ronanki, S. A. Singh, and S. S. Williamson, "Comprehensive topological overview of rolling stock architectures and recent trends in electric railway traction systems," *IEEE Trans. Transport. Electrific.*, vol. 3, no. 3, pp. 724–738, Sept 2017.

[16] A. Poorfakhraei, M. Narimani, and A. Emadi, "A review of modulation and control techniques for multilevel inverters in traction applications," *IEEE Access*, vol. 9, pp. 24 187–24 204, 2021.

[17] C. A. Reusser, H. A. Young, J. R. Perez Osses, M. A. Perez, and O. J. Simmonds, "Power electronics and drives: Applications to modern ship propulsion systems," *IEEE Ind. Electron. Mag.*, vol. 14, no. 4, pp. 106–122, Dec 2020.

[18] J. I. Leon, S. Vazquez, and L. G. Franquelo, "Multilevel converters: Control and modulation techniques for their operation and industrial applications," *Proc. IEEE.*, vol. 105, no. 11, pp. 2066–2081, Nov 2017.

[19] A. Dekka, B. Wu, R. L. Fuentes, M. Perez, and N. R. Zargari, "Evolution of topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 4, pp. 1631–1656, Dec 2017.

[20] F. Wang, "Motor shaft voltages and bearing currents and their reduction in multilevel medium-voltage pwm voltage-source-inverter drive applications," *IEEE Trans. Ind. Appl.*, vol. 36, no. 5, pp. 1336–1341, Sept 2000.

[21] J. Kalaiselvi and S. Srinivas, "Bearing currents and shaft voltage reduction in dual-inverter-fed open-end winding induction motor with reduced cmv pwm methods," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 144–152, Jan 2015.

[22] M. Hiller, R. Sommer, and M. Beuermann, "Medium-voltage drives," *IEEE Ind. Appl. Mag.*, vol. 16, no. 2, pp. 22–30, Mar-Apr 2010.

[23] H. Abu-Rub, S. Bayhan, S. Moinoddin, M. Malinowski, and J. Guzinski, "Medium-voltage drives: Challenges and existing technology," vol. 3, no. 2, pp. 29–41, Jun 2016.

[24] A. Muetze and C. R. Sullivan, "Simplified design of common-mode chokes for reduction of motor ground currents in inverter drives," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2570–2577, Nov-Dec 2011.

[25] H. Akagi and T. Shimizu, "Attenuation of conducted emi emissions from an inverter-driven motor," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 282–290, Jan 2008.

[26] C.-C. Hou, C.-C. Shih, P.-T. Cheng, and A. M. Hava, "Common-mode voltage reduction pulsewidth modulation techniques for three-phase grid-connected converters," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1971–1979, Apr 2013.

[27] V. Yaramasu, B. Wu, M. Rivera, M. Narimani, S. Kouro, and J. Rodriguez, "Generalised approach for predictive control with common-mode voltage mitigation in multilevel diode-clamped converters," *IET Power Electron.*, vol. 8, no. 8, pp. 1440–1450, Jul 2015.

[28] B. Horvath, "How isolation transformers in mv drives protect motor insulation," *TM GE Automation Systems, Roanoke, VA*, 2004.

[29] M. Verma, N. Bhatia, S. D. Holdridge, and T. O'Neal, "Isolation techniques for medium-voltage adjustable speed drives: Drive topologies for maintaining line-side performance," *IEEE Ind. Appl. Mag.*, vol. 25, no. 6, pp. 92–100, Nov-Dec 2019.

[30] N. Zhu, J. Kang, D. Xu, B. Wu, and Y. Xiao, "An integrated ac choke design for common-mode current suppression in neutral-connected power converter systems," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1228–1236, Mar 2012.

[31] N. O. Cetin and A. M. Hava, "Compatibility issues between the filter and pwm unit in three-phase ac motor drives utilizing the pure sine filter configuration," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2559–2569, Nov-Dec 2011.

[32] D. Jiang, F. Wang, and J. Xue, "Pwm impact on cm noise and ac cm choke for variable-speed motor drives," *IEEE Trans. Ind. Appl.*, vol. 49, no. 2, pp. 963–972, Mar-Apr 2013.

[33] J. Huang and H. Shi, "A hybrid filter for the suppression of common-mode voltage and differential-mode harmonics in three-phase inverters with cppm," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 3991–4000, Jul 2015.

[34] M. Mechlinski, S. Schröder, J. Shen, and R. W. De Doncker, "Grounding concept and common-mode filter design methodology for transformerless mv drives to prevent bearing current issues," *IEEE Trans. Ind. Appl.*, vol. 53, no. 6, pp. 5393–5404, Nov-Dec 2017.

[35] D. Han, F. Z. Peng, and S. Dwari, "A multilevel active cm noise power filter for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 70, no. 6, pp. 5454–5462, Jun 2023.

[36] M. Di Piazza, G. Tine, and G. Vitale, "An improved active common-mode voltage compensation device for induction motor drives," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1823–1834, Apr 2008.

[37] X. Chen, D. Xu, F. Liu, and J. Zhang, "A novel inverter-output passive filter for reducing both differential- and common-mode dv/dt at the motor terminals in pwm drive systems," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 419–426, Feb 2007.

[38] K. J. Dagan, A. Zuckerberger, and R. Rabinovici, "Fourth-arm common-mode voltage mitigation," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1401–1407, Jun 2016.

[39] J. I. Leon, S. Kouro, L. G. Franquelo, J. Rodriguez, and B. Wu, "The essential role and the continuous evolution of modulation techniques for voltage-source inverters in the past, present, and future power electronics," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2688–2701, May 2016.

[40] Y. Li, F. Diao, and Y. Zhao, "Simplified two-stage model predictive control for a hybrid multilevel converter with floating h-bridge," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4839–4850, Apr 2021.

[41] Y. Yang, H. Wen, M. Fan, M. Xie, S. Peng, M. Norambuena, and J. Rodriguez, "Computation-efficient model predictive control with common-mode voltage elimination for five-level anpc converters," *IEEE Trans. Transport. Electrific.*, vol. 6, no. 3, pp. 970–984, Sept 2020.

[42] R. M. Tallam, D. Leggate, D. W. Kirschnik, and R. A. Lukaszewski, "Reducing common-mode current: A modified space vector pulsewidth modulation scheme," *IEEE Ind. Appl. Mag.*, vol. 20, no. 6, pp. 24–32, 2014.

[43] M. Renge and H. Suryawanshi, "Five-level diode clamped inverter to eliminate common mode voltage and reduce dv/dt in medium voltage rating induction motor drives," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1598–1607, Jul 2008.

[44] B. Gutierrez, S. Baek, and J.-S. Lai, "Space vector pulsewidth modulation based on a novel digital coordinate transformation for multilevel inverters eliminating common-mode voltages," *IEEE Trans. Ind. Electron.*, pp. 1–11, 2024.

[45] L. Xu and Z. Q. Zhu, "Novel svpwm for open winding pmsm drives with simultaneous common mode voltage control and full frequency zero sequence current suppression," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 2, pp. 2151–2163, Apr 2023.

[46] J. Rodriguez, C. Garcia, A. Mora, S. A. Davari, J. Rodas, D. F. Valencia, M. Elmorshedy, F. Wang, K. Zuo, L. Tarisciotti, F. Flores-Bahamonde, W. Xu, Z. Zhang, Y. Zhang, M. Norambuena, A. Emadi, T. Geyer, R. Kennel, T. Dragicevic, D. A. Khaburi, Z. Zhang, M. Abdelrahem, and N. Mijatovic, "Latest advances of model predictive control in electrical drives–part ii: Applications and benchmarking with classical control methods," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5047–5061, May 2022.

[47] V. Yaramasu and B. Wu, *Model predictive control of wind energy conversion systems*. Hoboken, NJ, USA: Wiley-IEEE Press, Dec 2016.

[48] X. Li, M. Xie, M. Ji, J. Yang, X. Wu, and G. Shen, "Restraint of common-mode voltage for pmsm-inverter systems with current ripple constraint based on voltage-vector mpc," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 4, no. 2, pp. 688–697, Apr 2023.

[49] K. K. Monfared, H. Iman-Eini, Y. Neyshabouri, and M. Liserre, "Model predictive control with reduced common-mode voltage based on optimal switching sequences for nested neutral point clamped inverter," *IEEE Trans. Ind. Electron.*, vol. 71, no. 1, pp. 27–38, Jan 2024.

[50] A. Dekka, B. Wu, V. Yaramasu, and N. R. Zargari, "Dual-stage model predictive control with improved harmonic performance for modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 10, pp. 6010–6019, Oct 2016.

[51] I. Harbi, J. Rodriguez, E. Liegmann, H. Makhamreh, M. L. Heldwein, M. Novak, M. Rossi, M. Abdelrahem, M. Trabelsi, M. Ahmed, P. Karamanakos, S. Xu,

T. Dragičević, and R. Kennel, "Model-predictive control of multilevel inverters: Challenges, recent advances, and trends," *IEEE Trans. Power Electron.*, vol. 38, no. 9, pp. 10 845–10 868, Sept 2023.

[52] A. Dekka, B. Wu, V. Yaramasu, R. L. Fuentes, and N. R. Zargari, "Model predictive control of high-power modular multilevel converters–an overview," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 168–183, March 2019.

[53] A. Salem, M. A. Abido, and F. Blaabjerg, "Common-mode voltage mitigation of dual t-type inverter drives using fast mpc approach," *IEEE Trans. Ind. Electron.*, vol. 69, no. 8, pp. 7663–7674, Aug 2022.

[54] H. Le, A. Dekka, and D. Ronanki, "Low switching frequency fcs-mpc technique for four-level inverters," in *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2023, pp. 3062–3068.

[55] H. Le, A. Dekka, D. Ronanki, and J. Rodriguez, "A new predictive current control with reduced current tracking error and switching frequency for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 38, no. 9, pp. 10 798–10 809, Sept 2023.

[56] A. Dekka, B. Wu, V. Yaramasu, and N. R. Zargari, "Model predictive control with common-mode voltage injection for modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1767–1778, March 2017.

[57] S. Vazquez, J. Rodriguez, M. Rivera, L. G. Franquelo, and M. Norambuena, "Model predictive control for power converters and drives: Advances and trends," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 935–947, Feb 2017.

[58] Y. Yang, R. Chen, M. Fan, Y. Xiao, X. Zhang, M. Norambuena, and J. Rodriguez, "Improved model predictive current control for three-phase three-level converters with neutral-point voltage ripple and common mode voltage reduction," *IEEE Trans. Energy Convers.*, vol. 36, no. 4, pp. 3053–3062, Dec 2021.

[59] D. Busse, J. Erdman, R. Kerkman, D. Schlegel, and G. Skibinski, "System electrical parameters and their effects on bearing currents," *IEEE Trans. Ind. Appl.*, vol. 33, no. 2, pp. 577–584, Mar-Apr 1997.

[60] Y. Xu, Z. Wang, Y. Shen, Z. Zou, and F. Deng, "An improved modulation scheme of isolated matrix converter for common-mode voltage reduction and dc-bias current mitigation," *IEEE Trans. Ind. Electron.*, pp. 1–10, 2023.

[61] M. Renge and H. Suryawanshi, "Three-dimensional space-vector modulation to reduce common-mode voltage for multilevel inverter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2324–2331, Jul 2010.

[62] D. Hyypio, "Mitigation of bearing electro-erosion of inverter-fed motors through passive common-mode voltage suppression," *IEEE Trans. Ind. Appl.*, vol. 41, no. 2, pp. 576–583, Mar-Apr 2005.

[63] B. Wu, S. Rizzo, N. Zargari, and Y. Xiao, "An integrated dc link choke for elimination of motor common-mode voltage in medium voltage drives," in *Conference Record of the 2001 IEEE Industry Applications Conference. 36th IAS Annual Meeting (Cat. No.01CH37248)*, vol. 3, 2001, pp. 2022–2027 vol.3.

[64] N. Zhu, D. Xu, B. Wu, N. Zargari, M. Kazerani, and F. Liu, "Common-mode voltage reduction methods for current-source converters in medium-voltage drives," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 995–1006, Feb 2013.

[65] A. S. Lock, E. R. C. da Silva, M. E. Elbuluk, and D. A. Fernandes, "An apf-occ strategy for common-mode current rejection," *IEEE Trans. Ind. Appl.*, vol. 52, no. 6, pp. 4935–4945, Nov-Dec 2016.

[66] M. L. Heldwein, H. Ertl, J. Biela, and J. W. Kolar, "Implementation of a transformerless common-mode active filter for offline converter systems," *IEEE Trans. Ind. Electron.*, vol. 57, no. 5, pp. 1772–1786, May 2010.

[67] S. Takahashi, S. Ogasawara, M. Takemoto, K. Orikawa, and M. Tamate, "Common-mode voltage attenuation of an active common-mode filter in a motor drive system fed

by a pwm inverter," *IEEE Trans. Ind. Appl.*, vol. 55, no. 3, pp. 2721–2730, May-Jun 2019.

[68] S. Wang, Y. Y. Maillet, F. Wang, D. Boroyevich, and R. Burgos, "Investigation of hybrid emi filters for common-mode emi suppression in a motor drive system," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 1034–1045, Apr 2010.

[69] W. Yao, H. Hu, and Z. Lu, "Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 45–51, Jan 2008.

[70] S. Du, A. Dekka, B. Wu, and N. Zargari, *Modular Multilevel Converters: Analysis, Control, and Applications.* Hoboken, NJ, USA: Wiley-IEEE Press, Feb 2018.

[71] A. Gupta and A. Khambadkone, "A space vector modulation scheme to reduce common mode voltage for cascaded multilevel inverters," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1672–1681, Sept 2007.

[72] C. Wang, Q.-C. Zhong, N. Zhu, S.-Z. Chen, and X. Yang, "Space vector modulation in the 45° coordinates α'β' for multilevel converters," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6525–6536, Jun 2021.

[73] A. Hava and E. Un, "Performance analysis of reduced common-mode voltage pwm methods and comparison with standard pwm methods for three-phase voltage-source inverters," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 241–252, Jan 2009.

[74] E. Un and A. Hava, "A near-state pwm method with reduced switching losses and reduced common-mode voltage for three-phase voltage source inverters," *IEEE Trans. Ind. Appl.*, vol. 45, no. 2, pp. 782–793, Mar 2009.

[75] D. Prajapati, A. Dekka, D. Ronanki, and J. Rodriguez, "High-performance sequential model predictive control of a four-level inverter for electric transportation applications," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 5, no. 1, pp. 253–262, Jan 2024.

[76] N. S. P. Musunuru and S. Srirama, "Cascaded predictive control of a single power supply-driven four-level open-end winding induction motor drive without weighting factors," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 3, pp. 2858–2867, Jun 2021.

[77] J. Rodriguez, C. Garcia, A. Mora, F. Flores-Bahamonde, P. Acuna, M. Novak, Y. Zhang, L. Tarisciotti, S. A. Davari, Z. Zhang, F. Wang, M. Norambuena, T. Dragicevic, F. Blaabjerg, T. Geyer, R. Kennel, D. A. Khaburi, M. Abdelrahem, Z. Zhang, N. Mijatovic, and R. P. Aguilera, "Latest advances of model predictive control in electrical drives–part i: Basic concepts and advanced strategies," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 3927–3942, Apr 2022.

[78] H. Le, A. Dekka, and D. Ronanki, "Model predictive control of a new five-level inverter for medium voltage applications," in *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2023, pp. 2597–2602.

[79] T. Dragičević and M. Novak, "Weighting factor design in model predictive control of power electronic converters: An artificial neural network approach," *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 8870–8880, Nov 2019.

[80] T. Liu, A. Chen, C. Qin, J. Chen, and X. Li, "Double vector model predictive control to reduce common-mode voltage without weighting factors for three-level inverters," *IEEE Trans. Ind. Electron.*, vol. 67, no. 10, pp. 8980–8990, Oct 2020.

[81] M. J. Duran, J. A. Riveros, F. Barrero, H. Guzman, and J. Prieto, "Reduction of common-mode voltage in five-phase induction motor drives using predictive control techniques," *IEEE Trans. Ind. Appl.*, vol. 48, no. 6, pp. 2059–2067, Nov-Dec 2012.

[82] M. Narimani, B. Wu, V. Yaramasu, and N. Reza Zargari, "Finite control-set model predictive control (fcs-mpc) of nested neutral point-clamped (nnpc) converter," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7262–7269, Dec 2015.

[83] A. Dekka and M. Narimani, "Capacitor voltage balancing and current control of a five-level nested neutral-point-clamped converter," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10 169–10 177, Dec 2018.

[84] A. Bahrami, M. Norambuena, M. Narimani, and J. Rodriguez, "Model predictive current control of a seven-level inverter with reduced computational burden," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5729–5740, Jun 2020.

[85] R. Vargas, J. Rodriguez, C. Rojas, and M. Rivera, "Predictive control of an induction machine fed by a matrix converter with increased efficiency and reduced common-mode voltage," *IEEE Trans. Energy Convers.*, vol. 29, no. 2, pp. 473–485, Jun 2014.

[86] S. C. Chapra, R. P. Canale *et al.*, *Numerical methods for engineers*. Mcgraw-hill New York, 2011, vol. 1221.