Investigation of Capacitor Voltage Balancing Issues in a Five-Level Inverter with Multicarrier Modulation Schemes

By

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

ABSTRACT

Five-level inverters are widely used in medium-voltage (MV) wind energy and electric drive systems. However, the use of a large number of components (including passive and active components) and complex control methods are the major issues in the existing inverters. Also, some of the inverters are difficult to control using multicarrier modulation schemes due to the lack of redundancy switching states. In this research work, a new five-level inverter is introduced for MV applications. The new inverter requires only flying capacitors and switching devices and has a low total component count. Also, it requires only a flying capacitor voltage balancing method to achieve a safe and reliable operation. Hence, the new inverter is cost-effective and has less control complexity compared with the existing inverter topologies. The flying capacitor's voltage in the new inverter is analysed with the help of charge-balance theory and established as a theoretical basis for the capacitor voltage balancing method. Through this analysis, a simple voltage balancing method is developed. The developed balancing method is further analyzed with the conventional multicarrier modulation schemes using MATLAB simulations at different operating scenarios. Also, a modified multicarrier modulation scheme is introduced to handle the new inverter operation at higher load power factors. Finally, the performance comparison of the conventional and modified multicarrier modulation schemes is presented.

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I would like to express my sincere gratitude to my supervisor, Dr. Apparao Dekka for providing his invaluable support, and guidance throughout this research work.

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LIST OF SYMBOLS

Symbol	Meaning
3ϕ	Three-Phase
L_f, L_d	Filter Inductors
C_f, C_d	Filter Capacitors
v_a, v_b, v_c	Phase-*a*, -*b* and -*c* voltages
v_{dc}	DC-bus voltage
v_{ca1}, v_{ca2}, v_{ca3}	Flying capacitor voltages of phase-*a*
v_{cb1}, v_{cb2}, v_{cb3}	Flying capacitor voltages of phase-*b*
S_{x1}, S_{x2}, S_{x3} ……S_{x8}	Semiconductor switches of phase-*x*
d_{x1}, d_{x2}	Diodes of phase-*x*
v_{Cx1}, v_{Cx2}, v_{Cx3}	Flying capacitor voltages of phase-*x*
C_{x1}, C_{x2}, C_{x3}	Capacitance of the flying capacitors in phase-*x*
i_{cx1}, i_{cx2}, i_{cx3}	Flying capacitor currents of phase-*x*
v_{xN}	AC output voltage with respect to the negative DC-bus terminal
S_x	Voltage level of phase-*x*
i_{Nx1}, i_{Nx2}	Neutral point currents of phase-*x*
I_{Nx1}, I_{Nx2}	Average neutral point currents of phase-*x*
N_{x1}, N_{x2}	Flying capacitors neutral points of phase-*x*
v_{xo}	AC output voltage of phase-*x* with respect to DC-bus midpoint
i_x	Load current of phase-*x*
C	Capacitance
v_{Cxj}	Flying capacitor voltage of j^{th} flying capacitor in phase-*x*
Δv_{Cxj}	Peak-to-peak flying capacitor voltage ripple of j^{th} flying capacitor in phase-*x*
ΔV_{Cx1}, ΔV_{Cx2}, ΔV_{Cx3}	Flying capacitor voltage deviation in phase-*x*

$v_{Cx1}, v_{Cx2}, v_{Cx3}$	Flying capacitor voltages in phase-x
C_{xj}	Capacitance of j^{th} flying capacitor in phase-x
θ_x	Phase angle of phase-x
f_{cr}	Carrier frequency
V_{cr}	Amplitude of carrier signal
v^*_x	Reference modulation signal of phase x
m_a	Modulation index
f_o	Output frequency
v_{ab}	Line-to-line voltage
T_s	Sampling period
μ	Micro
C_1, C_2, C_3, C_4	Carrier Signals
V_{ref}	Reference modulating signal
V_{rip}	Flying capacitor voltage ripple
V_{THD}	Total harmonic distortion of voltage
I_{THD}	Total harmonic distortion of current
x	Phase terminal $x \in \{a, b, c\}$

LIST OF ABBREVIATIONS

Abbreviations	Meaning
MW	Mega Watt
MV	Medium Voltage
kV	Kilo-volt
F	Farad
Hz	Hertz
MLI	Multilevel Inverter
DC	Direct Current
NPV	Neutral-Point Voltage
PWM	Pulse Width Modulation
CSC	Current Source Converter
HVDC	High-Voltage Direct Current
VSC	Voltage Source Converter
WECS	Wind Energy Conversion System
PV	Photovoltaic
SCIG	Squirrel-Cage Induction Generator
PMSG	Permanent Magnet Synchronous Generator
WRSG	Wound Rotor Synchronous Generator
AC	Alternating Current
MSC	Machine Side Converter
GSC	Grid Side Converter
2L-VSC	Two-Level Voltage Source Converter
LC	Load Commutated
CMV	Common Mode Voltage
MVA	Mega-Volt-Ampere
5L	Five-Level

DCC	Diode Clamped Converter
SVM	Space Vector Modulation
FCC	Flying Capacitor Converter
ANPC	Active Neutral Point Clamped
HNPC	H-bridge/Neutral Point Clamped
HC	Hybrid Converter
MMC	Modular Multilevel Converter
SM	Submodule
HV	High Voltage
NNPC	Nested Neutral Point Clamped
CHB	Cascaded H-Bridge
SHE	Selective Harmonic Elimination
PSC-PWM	Phase Shifted Carrier PWM
LSC-PWM	Level Shifted Carrier PWM
PD-PWM	Phase-Disposition Pulse Width Modulation
POD-PWM	Phase Opposition Disposition PWM
APOD-PWM	Alternative Phase Opposition Disposition PWM
IGBT	Insulated-Gate Bipolar Transistor
SCMC	Series Connected Multilevel Converter
SMC	Stacked Multicell
NNPP	Nested Neutral-Pilot Point
NDC	Nested Diode Clamped
THD	Total Harmonic Distortion
COPWM	Carrier Overlap PWM
PF	Power Factor

CHAPTER 1

INTRODUCTION

1.1 MOTIVATION AND BACKGROUND:

In recent years, the power capacity of industrial systems is continuously growing with modernization and a rise in production demand. High-power inverters are highly needed to handle the increased power capacity in industrial systems. Currently, these inverters dominate the market up to a power capacity of 25 MW [1]. The high-power inverters are designed to operate at medium-voltage (MV) level of 3.3-6.6 kV to reduce the magnitude of the operating current, thereby the inverter power losses. To achieve the MV operation, the inverters are designed with low/medium/high voltage semiconductor devices [2].

The two-level inverters are highly mature and widely used in various power conversion systems. These inverters use medium or high-voltage switching devices and are connected in series to handle the MV operation. This process leads to a need for voltage equalization circuits to ensure equal blocking voltage across each switching device [3]. Furthermore, the two-level inverters require additional harmonic filters to improve the harmonic performance, which may cause resonance problems in the system.

On the contrary, the multilevel inverters (MLIs) generate a stepped voltage at the output leading to a significant reduction in the harmonics compared with the two-level inverters [4]. Also, the MLIs can be designed with low-voltage switching devices to handle the MV operation. Moreover, the realization of MLIs does not require the series connection of switching devices, which results in the elimination of the voltage equalization circuits. However, the MLIs require higher active and passive components, and a complex control system to manage multiple control objectives [5].

Even though several MLIs have been developed over the years, the researchers are still focusing on the improvement of the power density, cost, control complexity, and reliability performance of the MLIs. Currently, five-level inverters have gained attention for 4.16 kV power conversion systems as they can easily meet the application requirements such as low common-mode voltage, low *dv/dt*, and low harmonic distortion [6]. However, the many newly developed five-level inverters need more flying capacitors

to achieve multilevel operation. These flying capacitors need a voltage control mechanism, and their complexity increases with the number of flying capacitors. Additionally, the reliability of inverters is impacted by the increase in the flying capacitors.

1.2 THESIS OBJECTIVES:

The existing MLIs require isolated DC sources, a large number of components (including passive and active components), and complex control methods to handle DC-bus neutral-point voltage (NPV) and flying capacitor's voltage balancing. Furthermore, some of the MLIs are difficult to control using the conventional multicarrier PWM schemes due to the lack of redundancy switching states. Also, the conventional multicarrier PWM schemes have limited flying capacitor voltage controllability under high-power factor operation. Considering these issues, the thesis research objectives are summarized as follows:

1) Development of five-level MLI with reduced component count for medium-voltage (MV) applications:

   A new five-level MLI will be introduced for MV applications. The new inverter does not require any clamping diodes and isolated DC sources. Also, the absence of DC-bus neutral points eliminates the need for a DC-bus NPV controller. Moreover, the net component count is much lesser than the existing five-level inverters. In the new inverter, the MLI operation will be achieved with the help of switching devices along with the flying capacitors only. The flying capacitor's voltage can be controlled with the help of redundancy switching states alone. Hence, it does not require a complex control system.

2) Investigation of flying capacitors voltage balancing issues in the new five-level MLI:

   The flying capacitor's voltage needs to be regulated at its rated value to generate high-quality output voltage and current waveforms while maintaining the switching device's voltage stress at its rated value. Hence, the flying capacitor voltage balancing is highly needed for the new five-level MLI to achieve a safe and reliable operation. To develop a flying capacitor voltage balancing method, a theoretical basis for the flying capacitor's voltage variation is established based on the charge-balance theory. Through this theory, the charging and discharging processes of the flying capacitors are analysed for different load

power factors. Also, the mathematical models are established to identify the control variables to achieve the flying capacitor's voltage balancing under a wide range of load power factors.

3) Investigation of multicarrier PWM schemes for the new five-level MLI under a wider range of load power factors:

   The conventional multicarrier PWM schemes are easy to implement and extend to higher-level MLIs compared with the SVM and SHE schemes. Hence, the conventional multicarrier PWM schemes including both LSC-PWM and PSC-PWM are considered for the new five-level inverter. The flying capacitor voltage balancing issues in the five-level inverter are further investigated with the conventional multicarrier PWM scheme through simulation studies. Also, a new modified multicarrier PWM scheme is proposed to handle the operation of the new five-level under a wide range of load power factors.

1.3 THESIS OUTLINE:

The research presented in this thesis is organized into four chapters. A brief description of each chapter is presented as follows:

- **Chapter 1 –** In this chapter, an introduction on the growing demand and need for multi-level inverters is described and the research objectives and outline of the thesis are presented.

- **Chapter 2 –** In this chapter, an introduction to the conventional five-level MLIs and their applications are described. Also, a brief description of the conventional PWM schemes is discussed.

- **Chapter 3 –** This chapter introduces a new five-level MLI for medium-voltage high-power applications. A comparative study of the new five-level MLI with the conventional five-level MLIs in terms of component count and control complexity is conducted. Also, the analysis of the flying capacitor's voltage variation with the charge-balance theory is assessed. Finally, a flying capacitor voltage balancing method is introduced for the new five-level inverter. The steady-state and transient performance of the voltage balancing method with the conventional LSC-PWM scheme is evaluated.

- **Chapter 4 –** In this chapter, the performance analysis of the five-level MLI with the PSC-PWM scheme is discussed. Also, the philosophy of the proposed modified multicarrier PWM scheme is introduced. Finally, the simulation studies under steady-state and transient conditions are presented. Also, the performance of the proposed PWM scheme is compared with the conventional multicarrier PWM schemes.

- **Chapter 5 –** The outcomes of the thesis work are summarized in this chapter. Additionally, the future directions of the presented thesis work are also suggested.

CHAPTER 2

OVERVIEW OF MULTILEVEL INVERTERS

The five-level multilevel inverters (5L-MLIs) are widely used in 4.16 kV power conversion systems. Over the years, several 5L-MLIs are developed focusing on the reduction of component count and control complexity. These pros and cons of the existing 5L-MLI topologies are summarized in this chapter. This chapter is structured as follows: Section 2.1 presents the applications of MLIs. Sections 2.2 and 2.3 provide an overview of traditional five-level inverter topologies and PWM schemes, respectively.

2.1 APPLICATIONS OF MLI:

In the early days, the current source converter (CSC) topologies have been found in various industrial applications including wind energy, motor drives, railway traction, and high-voltage direct current (HVDC) transmission systems. However, the total adoption of CSC in the industry has been limited by various issues involving the need for a bulky DC-link inductor, a complex gating circuit, and a poor transient response [7]. Alternatively, voltage source converters (VSCs) became popular with the advent of fast-acting switching devices. Thereby, the VSC topologies have superior transient response and ease of control with a simple gating circuit compared with the CSC topologies.

The two-level inverter is one of the basic and highly matured VSC technologies. It is widely used in applications with a voltage rating of less than 1 kV. For operating voltages greater than 1 kV, the two-level inverter is less attractive due to the need for harmonic filters, *dv/dt* filters, and series connection of high voltage switching devices. The MLIs became an alternative for two-level inverters to handle higher operating voltages. Furthermore, these inverters have superior harmonic performance and low *dv/dt* compared with the two-level inverters. Some of the popular applications of MLIs are wind energy conversion systems (WECS), MV motor drives, and photovoltaic (PV) energy systems [7].

2.1.1 Wind Energy Conversion System:

Wind energy has become the world's fastest-growing renewable energy source, with an average growth rate of 21% over the past decade [7]. This has boosted the demand for improved WECS to harvest more energy from the wind. Currently, the wind energy industries have reported a growth rate of more than 19%, accounting for 1.9% of global net power output [8]. The wind energy industry has undergone many technological advancements in terms of mechanical systems, electric generators, power converters, and control methods.

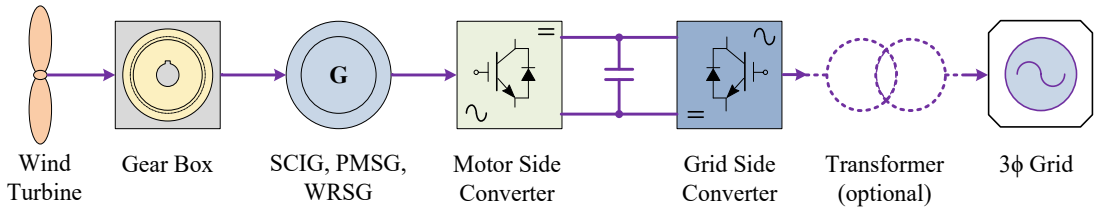


Fig. 2.1: Basic configuration of grid-connected wind energy conversion system.

The configuration of grid-connected WECS is shown in Fig. 2.1. In which, the generators and power converters are the critical components of WECSs from the electrical engineering standpoint. The generator, in general, is used to transform mechanical energy into electric energy. The first-generation WECSs are designed with a squirrel-cage induction generator (SCIG) for both fixed and variable-speed operation. Typically, these generators are designed with fewer poles leading to higher rotational speeds. Therefore, the SCIG-based WECS requires a gearbox to match the low-speed wind turbine and high-speed generator shaft. However, the use of a gearbox reduces the reliability of the WECS due to the higher chance of its failure [8]. Alternatively, the WECS is designed with permanent magnet synchronous generators (PMSG) and wound rotor synchronous generators (WRSG). Among them, the PMSG-based WECS became popular due to the gear-less operation, higher energy conversion efficiency, and ease of control [8], [9].

The generator's electrical power output erratically fluctuates, and its frequency varies with the wind speed. Hence, a power conversion system is required to convert its frequency equivalent to the grid frequency while minimizing the power fluctuations to meet the grid codes [9]. Typically, the power conversion process takes place in two stages as shown in Fig. 2.1. In the first stage, the variable frequency AC power is converted into DC power by using a machine-side converter (MSC). The DC power is converted into constant frequency AC power by using a grid-side converter (GSC). Different topologies

are available in the literature to realize both MSC and GSC systems [10]. Depending on the topology, the WECS may need harmonic filters to minimize the *dv/dt* and harmonics. A step-up transformer can be used if the power converter is unable to operate at the voltage level requirement of the grid side.

2.1.2 Photovoltaic Energy System:

The photovoltaic (PV) energy system installations have grown annually at a 60% pace over the past five years, outpacing one-third of total wind energy installed capacity [11],[12]. The PV systems are available in both standalone and grid-connected configurations. However, grid-connected systems account for roughly 90% of all PV systems installed around the globe [11]. The configuration of a grid-connected PV system is shown in Fig. 2.2, in which the solar cell, power converters (including PV-side converter and grid-side converter), and utility grid are the fundamental components.

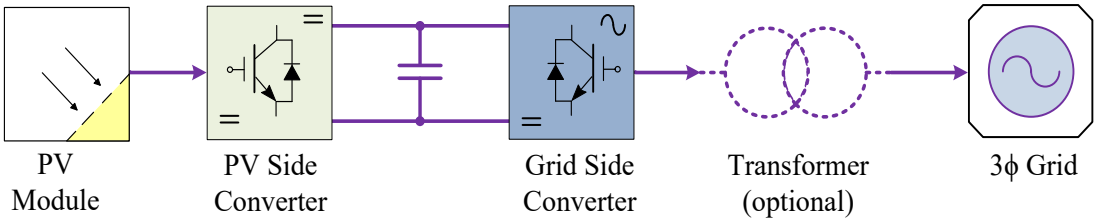


Fig. 2.2: Basic configuration of a grid-connected PV system.

The PV panels are designed with the interconnection of multiple solar cells, which converts the solar irradiance into DC power. This DC power is produced at low current and low voltage, which is further boosted to a high voltage DC power using a PV-side converter (DC boost converter). This power is converted into AC power at grid frequency and supplied to the utility grid [12]. The designed power converter system should meet both grid and safety codes such as low leakage current, high power factor operation, and low harmonic distortion [11]-[14].

2.1.3 Motor Drive System:

The MLIs can also be found in medium-voltage (MV) motor drive systems. The MV motor drives are widely used in the energy, transportation, mining, pulp/paper, and water treatment industries. These drives are available with a power rating of 0.4-40 MW

and a voltage rating of 2.3-13.8 kV as shown in Fig. 2.3 [2], [3]. However, MV drives with a power rating of 1-4 MW and voltage rating of 3.3-6.6 kV are dominated in a wide range of commercial applications. Some critical applications of MV drives are fans, pumps, conveyors, and compressors [5].

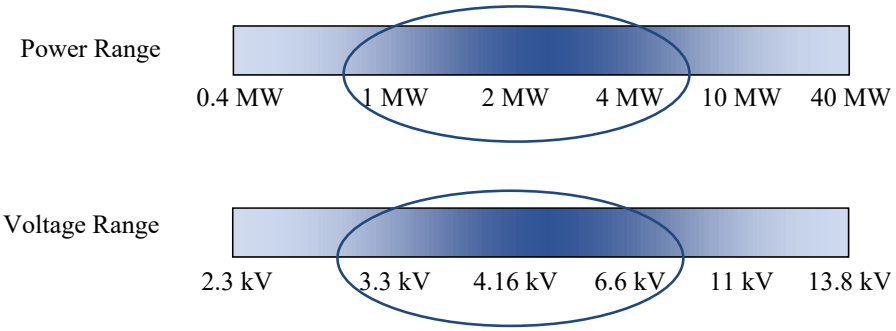


Fig. 2.3: Voltage and power ranges of MV motor drives [4].

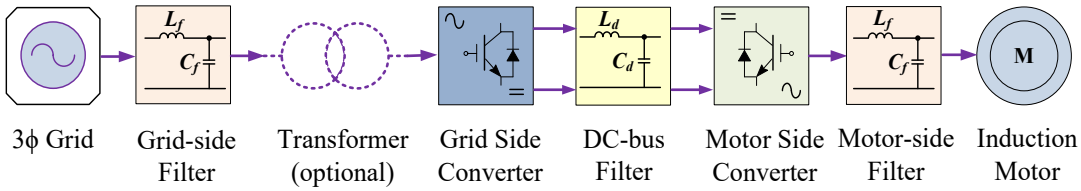


Fig. 2.4: Basic configuration of MV motor drive.

Fig. 2.4 depicts a typical MV motor drive system, which includes AC grid mains, transformer, power converters, filters, and motor. The transformer helps to step down the AC grid voltage to the converter operating working voltage and provides galvanic isolation. The filters on the motor and grid side are optional, and they are used to reduce the harmonic distortion and *dv/dt* [5], [15]. A phase-shifting transformer can also be used to minimize the lower-order harmonics on the grid side as per the IEEE-519 harmonic standards and block the drive common-mode current [15], [16].

In the motor drive system, the power conversion takes place in two stages. In the first stage, the AC grid power at constant frequency is converted into DC power using an active or passive front-end rectifier system. The DC-bus filter is used to suppress the DC power fluctuations. This filter will be realized with an inductor in the CSC system, whereas the capacitor is used in the VSC system. The DC power is converted back to AC power at variable frequency, and it is fed to the motor as shown in Fig. 2.4. The grid-side converter regulates DC-bus voltage while controlling the grid power factor, whereas the

motor-side converter controls the motor flux and torque/speed [5], [15]. Overall, the power converters are the heart of the MV motor drive system. Therefore, the topology selection, design, and control play a significant role in achieving a high-efficiency drive system. Moreover, these power converters should meet the operating requirements of the application, such as high-power factor and variable speed operation.

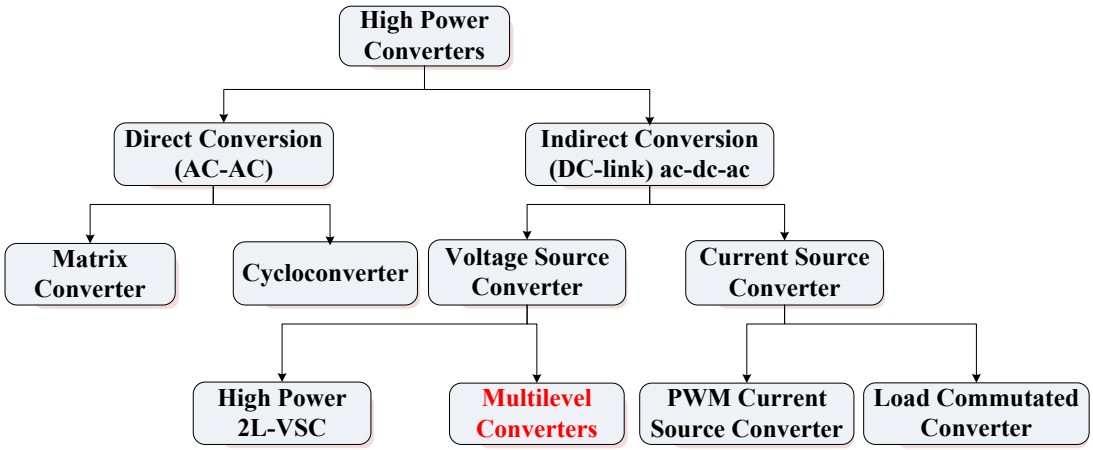


Fig. 2.5: Classification of high-power converters.

2.2 CLASSIFICATION OF MLIS:

Power converters play a critical role in shaping the market for MV applications and meeting the world's energy demand. Several industrial manufacturers have joined the MV market, offering a diverse range of high-power converter topologies. These converter topologies are categorized into two groups based on the power conversion stages involved between the source and the load, and they are named as direct power conversion and indirect power conversion [17]. In the direct power conversion process, the AC power at a fixed frequency is directly converted to AC power at a variable frequency. This process involves only a single stage and does not require any DC energy storage link between the source and the load. The indirect power conversion process involves two stages named AC-DC conversion (rectification) and DC-AC conversion (inversion) stages. In the AC-DC conversion stage, the AC power at a fixed frequency is converted into DC power, whereas the DC power is converted into AC power at a variable frequency in the DC-AC conversion stage [17]. The two-stage power conversion needs a DC energy storage link between the rectification and inversion stages. Depending on the type of DC energy

storage link, the indirect conversion is further classified into voltage and current source converters based on the DC energy storage link as illustrated in Fig. 2.5.

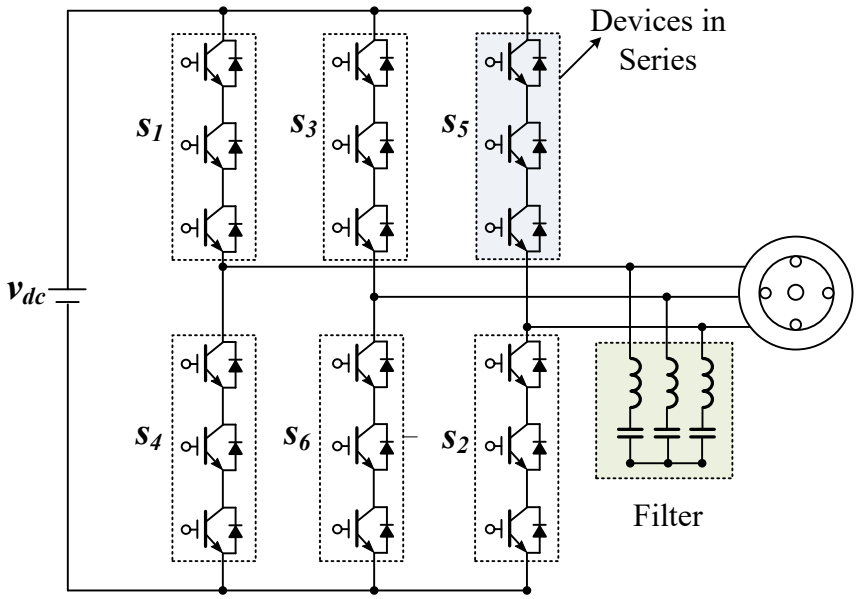


Fig. 2.6: Two-level voltage source converter [4].

In comparison to current source converter (CSC) topologies, voltage source converters (VSC) have had a higher market penetration and more noticeable development over the last decade [6]. The prominent features of the VSCs are high-power quality, fast dynamic response, high efficiency, and reliability, making the VSC fulfil many challenges in medium-voltage applications. The evolution of VSC began with the advent of two-level VSC (2L-VSC), which was used primarily in low voltage, low-power applications as shown in Fig. 2.6. For high-power applications, the 2L-VSC needs to handle low current at medium-voltage level or high current at low voltage level. However, the low current operation is highly preferred due to the low system power losses and the smaller size of the required conductor. Considering the available semiconductor devices, the 2L-VSC needs the series connection of switching devices to handle the low current at a medium voltage level [17]. However, the series connection of devices causes unequal blocking voltage stress due to the delay in switching action, which further leads to their failure over the long run. Hence, the 2L-VSC requires additional voltage equalization circuits, which will further increase losses in the system [5]. Also, the 2L-VSC needs an LC filter at the load side to minimize the harmonic distortion and dv/dt stress. These filters cause LC resonance problems, which will worsen the load performance.

As a result, multilevel converters were developed, which produce staircase voltage waveforms at the output. The voltage and current harmonic distortion can be minimized by raising the output voltage levels. A three-level inverter initially presented in 1981 [18] was the first multilevel converter. The invention of multilevel converters has decreased the requirement for expensive semiconductor devices and the need for device series connections. Additionally, the multilevel converter offers low *dv/dt*, low common-mode voltage (CMV), high efficiency, and the elimination of the output filters [19]. The most prominent characteristics of the multilevel converter are [20]:

1) Output voltage with low harmonic distortion and low *dv/dt*.
2) Draws the current with low harmonic distortion.
3) Reduced CMV, thus, minimizes the voltage/current stress on bearings,
4) Can operate with low switching frequency leading to low switching losses and higher efficiency.

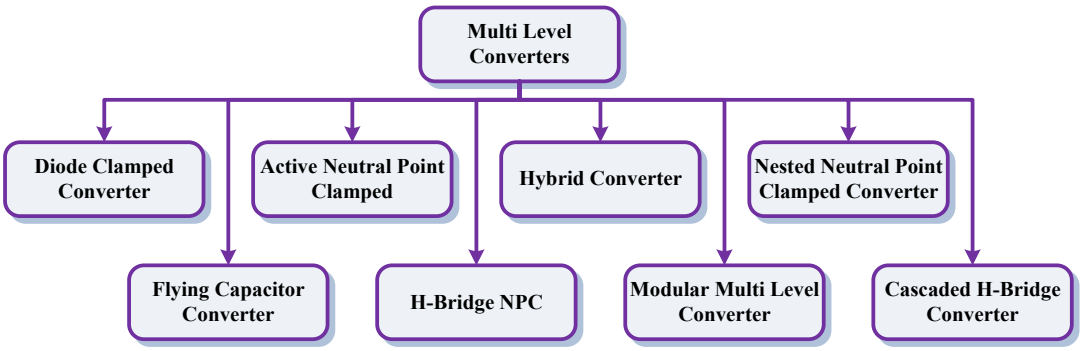


Fig. 2.7: Classification of multilevel converters.

Over the years, several multilevel converters have been developed for high-power applications. Some of the popular multilevel converters are depicted in Fig. 2.7. These converters are available in different output levels to handle an operating voltage of 2.3-13.8 kV and a power capacity of 0.3 to 32 MVA [21], [22],[23]. The selection of topology depends on the operating voltage, available semiconductor devices, cost, reliability, size, control complexity, efficiency, and harmonic distortion. This thesis focuses on the five-level (5L) operation of multilevel converters, and their limitations and challenges for MV applications.

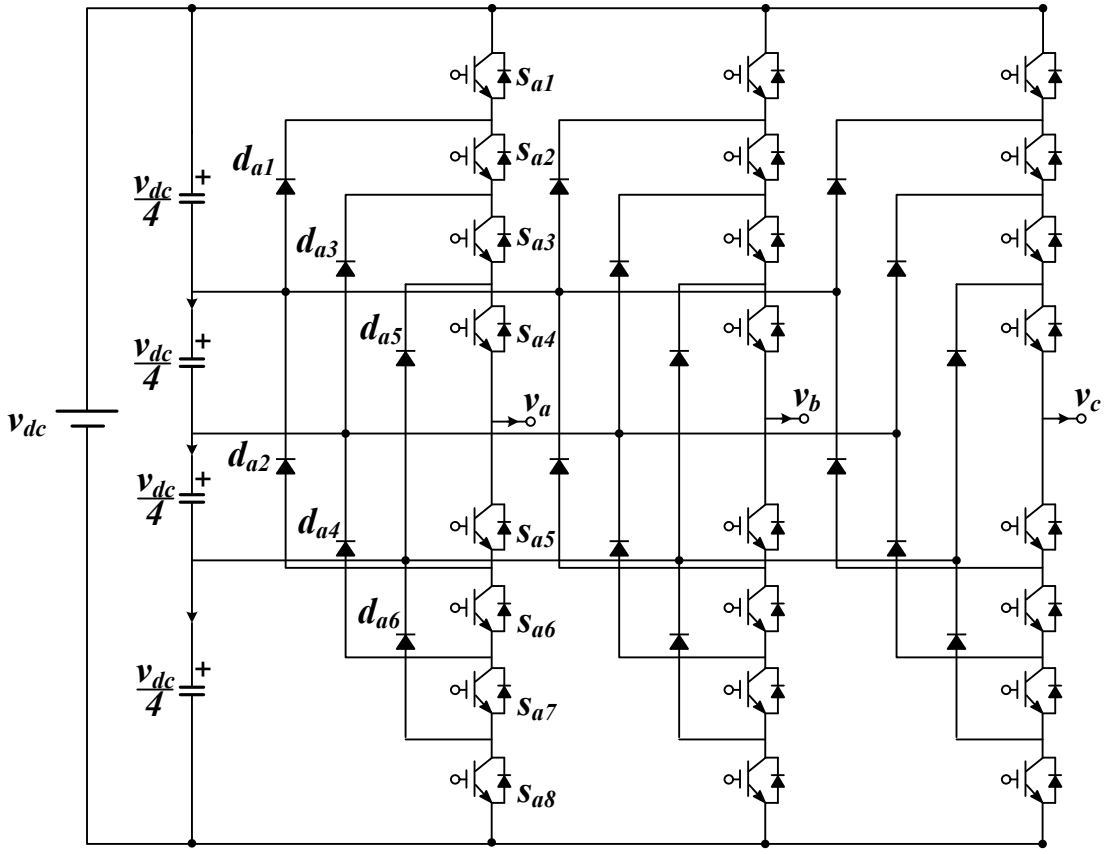


Fig. 2.8: Five-level DCC [24].

2.2.1 Diode Clamped Converter:

The three-phase circuit configuration of a five-level diode clamped converter (5L-DCC) is shown in Fig. 2.8. This converter requires a total of 24 switching devices and 36 clamping diodes of $v_{dc}/4$ rating each, where v_{dc} is the DC-bus voltage. The switching devices in each leg are clamped to the DC-bus neutral-point voltage through the clamping diodes, thereby each device will experience a blocking voltage of $v_{dc}/4$ as shown in Fig. 2.8 [24]. The DCC requires a large number of clamping diodes which leads to increased complexity in the assembly and manufacturing process of the converter. Furthermore, the DCC has multiple DC-bus neutral points, and their voltage needs to be regulated at $v_{dc}/4$ each [25]. However, due to the lack of redundancy switching states, it is difficult to achieve the DC-bus neutral-point voltage (NPV) control using multicarrier pulse width modulation (PWM) schemes [26]. Alternatively, complex space vector modulation (SVM) schemes are presented to control the 5L-DCC. However, these methods are challenging to put into practice due to the complexity of identifying and selecting switching vectors, computing duty cycles, and selecting switching sequences [27]. Also,

the unequal conduction and switching losses lead to unequal device power losses, which causes thermal problems in the DCC [27]. Hence, the DCC applications are limited to three-level operations only.

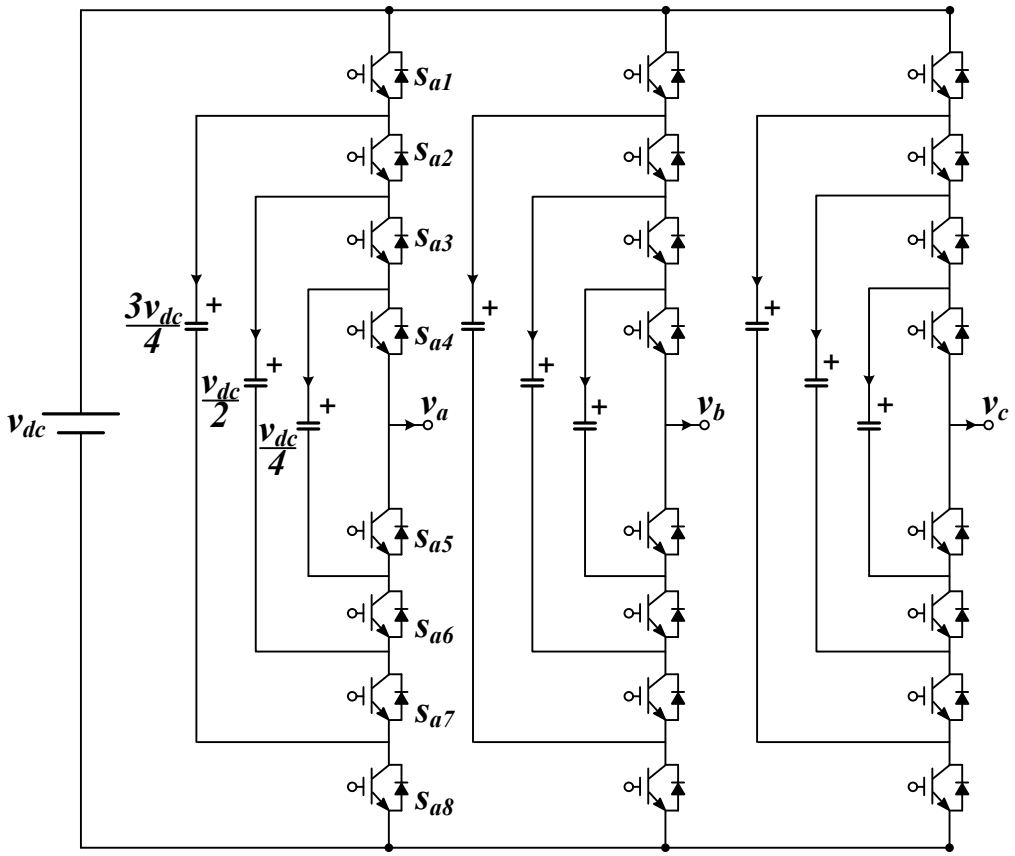


Fig. 2.9: Structure of 5L-FCC [4].

2.2.2 Flying Capacitor Converter:

The Flying capacitor concept was introduced in the early 1970s [28]. Fig. 2.9 shows the structure of a three-phase five-level flying capacitor converter (5L-FCC). The FCC necessitates 24 switching devices and 18 flying capacitors of $v_{dc}/4$ voltage rating each and also eliminates the clamping diodes and DC-bus neutral points compared with the DCC [29]. Furthermore, the multilevel operation is achieved by using the flying capacitors only. Hence, it requires the flying capacitor's voltage control mechanism only. However, the use of more flying capacitors leads to the poor reliability of the converter.

Additionally, the flying capacitors require pre-charging circuits since they have zero initial voltage and must be charged during the start-up process [28]. Also, during

low-frequency operations, the 5L-FCC produces large capacitor voltage ripples. Therefore, they must either increase their switching frequencies or design with a large capacitance to manage their ripples. [30]. In addition to the ripple minimization, the flying capacitor's voltage needs to regulate at its rated value. In order to achieve this objective, a combination of voltage balancing methods and phase-shifted carrier PWM techniques are utilized [31]. These methods are designed to select the proper switching state from the redundancy based on the current direction, capacitor voltage deviation, and voltage level [32]. Even though these methods are straightforward to implement, the large capacitor voltage ripple, converter reliability, and need for pre-charging circuits have limited their practical feasibility for industrial applications.

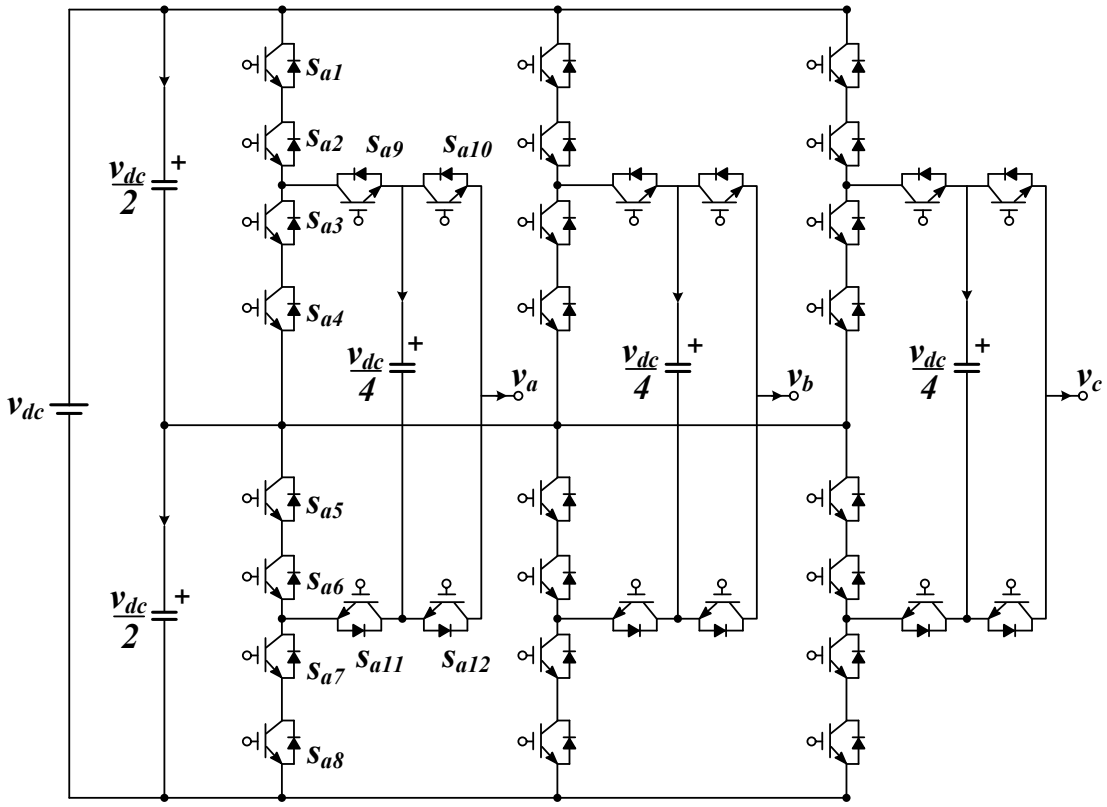


Fig. 2.10: Structure of 5L-ANPC [33].

2.2.3 Active Neutral Point Clamped:

The structure of a three-phase five-level active neutral-point clamped (5L-ANPC) converter is shown in Fig. 2.10. It is designed with a combination of three-level ANPC and a flying capacitor cell. The 5L-ANPC requires 36 switching devices and 6 flying

capacitors of $v_{dc}/4$ voltage rating each [33]. Compared with the DCC and FCC, the ANPC requires more switching devices and fewer flying capacitors. Also, the DCC requires a DC-bus neutral-point voltage control along with the flying capacitor voltage control. Hence, the overall control complexity of the 5L-ANPC is relatively high compared with other topologies. Furthermore, the ANPC requires multiple voltage equalization circuits due to the multiple series connection of multiple switching devices, which further increases the complexity of the topology control. This converter covers applications with a power range of 20-200 MVA [6]. Unlike the DCC, the active switching devices are used to clamp the DC-bus mid-point in the ANPC. This will further provide a controlled current path to adjust uniform loss distribution between the switching devices compared with the DCC [34].

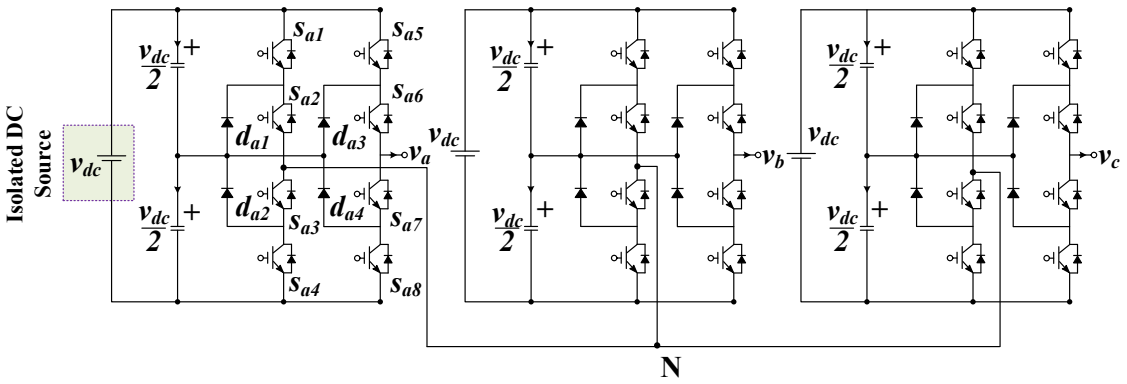


Fig. 2.11: Structure of 5L-HNPC [35].

2.2.4 H-bridge/Neutral-Point Clamped Converter:

The structure of a three-phase five-level H-bridge/neutral-point clamped converter (5L-HNPC) is shown in Fig. 2.11. This topology is first proposed for a motor drive application [35], and it is composed of 2 three-level DCC modules joined together to form an H-bridge as shown in Fig. 2.11. The 5L-HNPC requires 24 switching devices and 12 clamping diodes. Even though the component count is much lesser compared with the DCC, FCC, and ANPC topologies, it requires an isolated DC source for each phase [35], [36]. To generate the isolated DC source, a phase-shift transformer with multiple secondary windings is required. The phase-shift transformer allows the cancellation of specific lower-order harmonics, thereby it helps in improving the grid power quality. However, the transformer increases the overall system cost and size. The use of

transformers affects the system efficiency as their power losses are accountable for 2% of the total system power losses [5]. Furthermore, the HNPC topology also requires a complex control system to control the neutral point voltage of each leg of the inverter [6].

2.2.5 Hybrid Converter:

The five-level hybrid converter (5L-HC) combines the structure of ANPC and FCC, and the resultant converter is shown in Fig. 2.12. The 5L-HC requires a total of 30 switching devices and 9 flying capacitors of $v_{dc}/4$ voltage rating each [37]. The DC-bus of the 5L-HC is divided into three parts; the top and lower DC-bus capacitors have a voltage rating of $v_{dc}/4$, whereas the middle DC-bus capacitor has a voltage rating of $v_{dc}/2$ [37]. Also, the 5L-HC uses more flying capacitors to eliminate the series connection of switching devices and the corresponding voltage equalization circuit [38]. Overall, the 5L-HC requires a DC-bus NPV along with a flying capacitor voltage control to achieve a reliable five-level operation. This process significantly increases the control complexity of the 5L-HC. Typically, the redundancy switching states are used to regulate the voltage of the flying capacitors, whereas the common-mode voltage will be injected into the system to handle the DC-bus NPV balancing [39]. The injected common-mode voltage increases the device's voltage stress and net common-mode voltage of the 5L-HC. The increased common-mode voltage further causes bearing failures in motor drive applications. Hence, the 5L-HC lacks commercial applications.

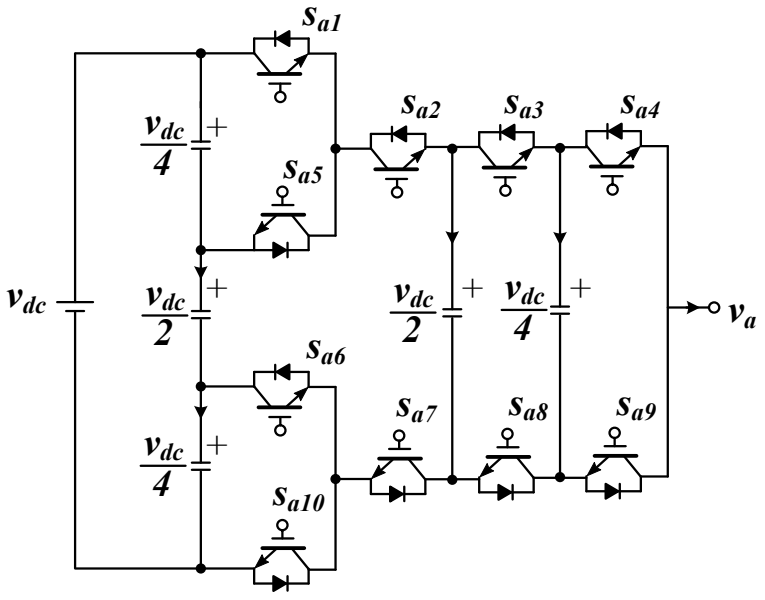


Fig. 2.12: Single-phase structure of 5L-HCC [37].

2.2.6 Modular Multilevel Converter:

The modular multilevel converter (MMC) architecture is well recognized for its use in high-voltage direct current (HVDC) systems and its structure is shown in Fig. 2.13. This topology was initially developed in the early 2000s for power-quality applications. Later, the MMC is further investigated for motor drives, large PV plants, and offshore wind farms [40],[41]. The MMC can operate in a wide range of voltages from the medium voltage (2.3-13.8 kV) to high voltage (33-400 kV), corresponding with a wide range of power ratings (0.0226-1000 MW). Modular architecture, voltage and power scaling, fault-tolerant operation with submodule (SM) redundancy, and direct connection to HV networks without line-frequency transformers are some of the eminent advantages of this topology [42]. Also, MMC enables the use of low-voltage semiconductors to achieve medium and high-voltage operation. Besides, the MMCs do not require a phase-shifting transformer, which can result in a reduction in the cost and size of the system [43].

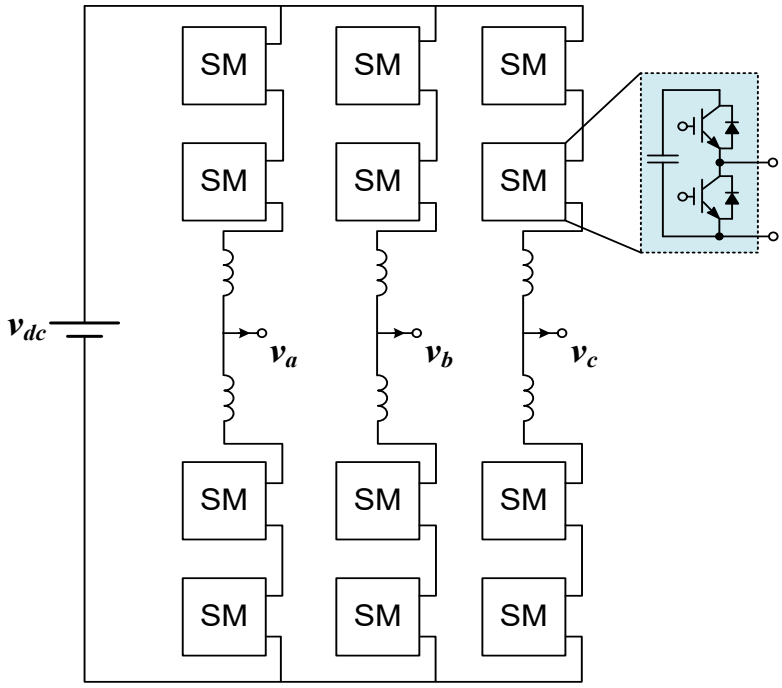


Fig. 2.13: Structure of MMC [42].

On the other hand, design constraints, submodule capacitor voltage control, circulating current, submodule capacitor voltage ripple, and submodule capacitor pre-charging process are the technical challenges associated with the operation and control of

MMCs. Moreover, the MMC requires a complex control system to achieve multiple control objectives [43]. Submodule structure also requires many components, which may increase the cost and affect the reliability of the system. Besides, when applied in medium-voltage motor drives, the MMC experiences low-frequency fluctuation in the flying capacitors [44]-[46]. Thus, it will not be feasible for constant torque loads that require the rated torque in a low-speed region.

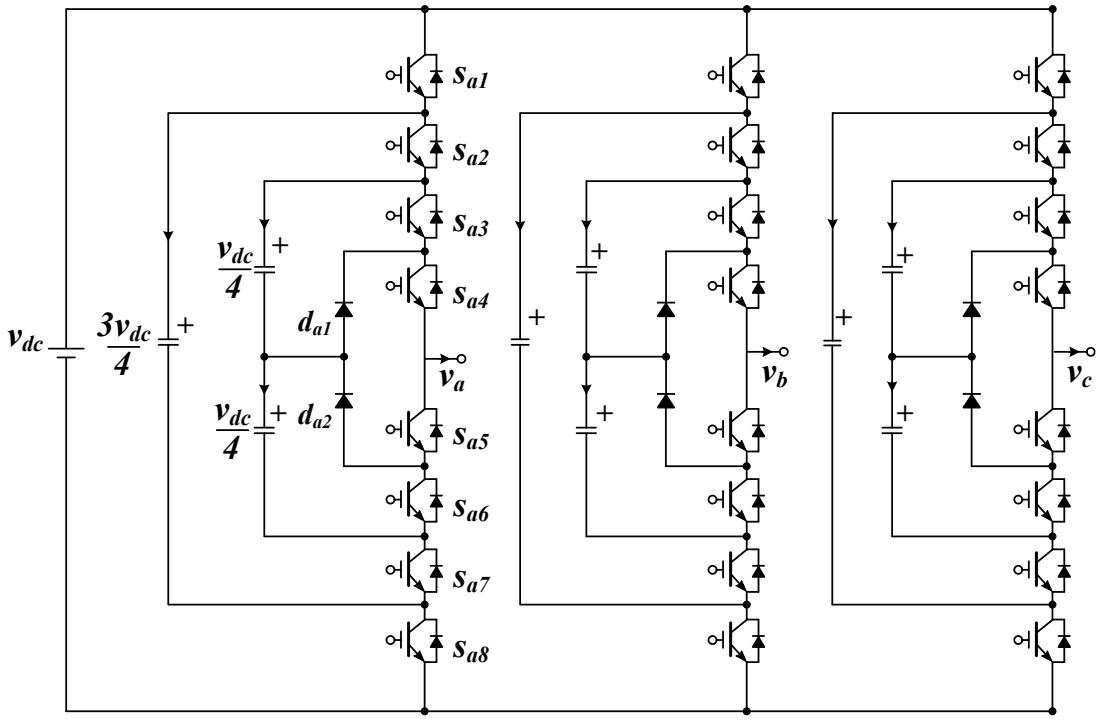


Fig. 2.14: Structure of 5L-NNPC [47].

2.2.7 Nested Neutral Point Clamped Converter:

The structure of a three-phase five-level nested neutral point clamped (5L-NNPC) converter is shown in Fig. 2.14. It is designed from a combination of DCC and FCC converters. In contrast to the DCC topology, the NNPC employs FCs, switching devices, and clamping diodes with identical voltage ratings. The NNPC topology requires a total of 24 switching devices, 6 clamping diodes, and 15 flying capacitors of $v_{dc}/4$ voltage rating each [47]. It also can reach an operating voltage of 2.3-6.6 kV. The NNPC converter has enough redundancy states, making the balancing of the flying capacitor's voltage with multicarrier PWM techniques easier. However, the use of many flying capacitors makes the topology bulky in size and affects the converter's reliability [47].

Also, the flying capacitors experience high ripples during low-frequency operation, making the topology less attractive for variable-speed applications.

2.2.8 Cascaded H-bridge Converter:

The cascaded H-bridge (CHB) converters are designed with a series connection of identical rating H-bridge modules as shown in Fig. 2.15. The CHB topology can reach an operating voltage of up to 13.8 kV and is widely used in motor drive applications. The operating voltage and output levels of the CHB topology can be easily increased by adding more H-bridge modules in series [4]. Furthermore, the CHB has a modular construction and allows fault-tolerant operation. Under fault conditions, the CHB topology can continue to operate with reduced power capacity, thereby significantly reducing the system downtime of the industrial processes. Also, the manufacturing, assembly, and maintenance cost of the CHB topology is relatively low compared with other existing MLIs [4]. However, the CHB topology requires a phase-shift transformer with multiple secondary windings to generate the isolated DC source for each H-bridge module [5]. Hence, the CHB is not cost-effective for an operating voltage of less than 6.6 kV.

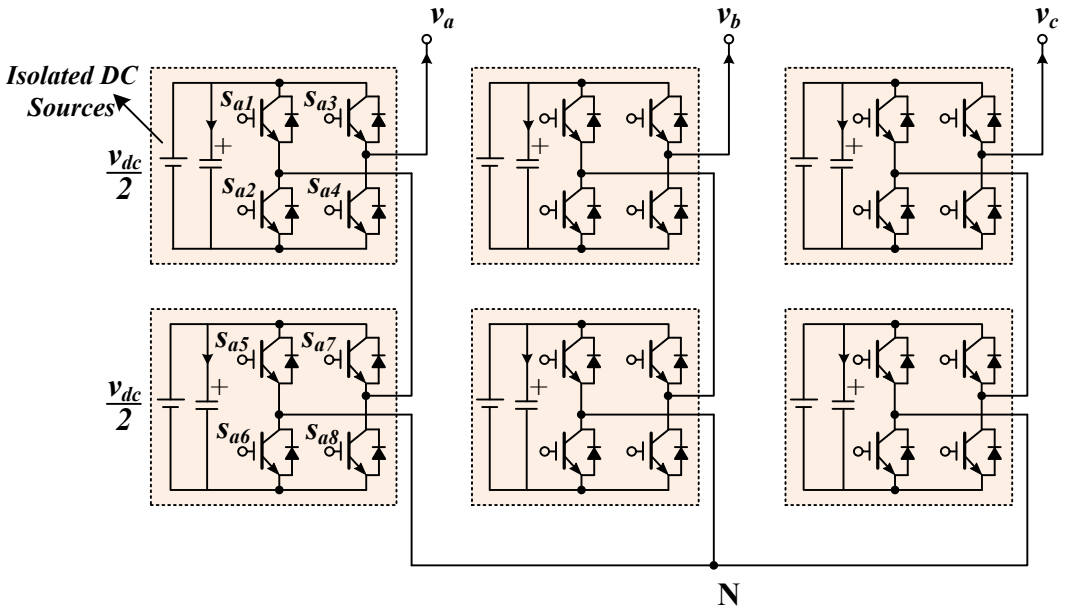


Fig. 2.15: Structure of CHB [4].

2.3 PULSE WIDTH MODULATION SCHEMES:

Pulse width modulation (PWM) schemes play a key role in generating the switching signals to the semiconductor devices used in the MLIs. Thereby, the stepped voltage waveform that closely matches the reference voltage will be produced at the output [6]. These modulation schemes are also designed to meet the application requirements such as low switching frequency operation, low harmonic distortion, and low common-mode voltage while fulfilling the system control objectives such as current tracking, flying capacitor's voltage control, and DC-bus NPV control [6], [22], [47]. Over the years, several PWM schemes have been developed to achieve a safe, reliable, and efficient operation of MLIs. These modulation schemes are broadly categorized into multicarrier modulation, space vector modulation (SVM), and selective harmonic elimination (SHE) schemes as shown in Fig. 2.16 [48], [49].

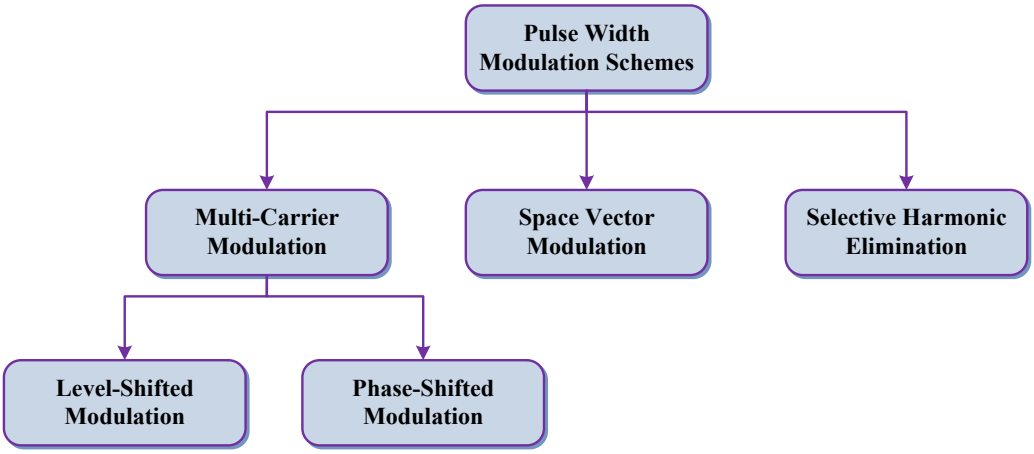


Fig. 2.16: Classification of PWM schemes.

Depending on the carrier arrangement, the multicarrier modulation schemes are further categorized into level-shifted carrier PWM (LSC-PWM) and phase-shifted carrier PWM (PSC-PWM) schemes as shown in Fig. 2.16. These schemes directly modulate each phase of the power converter independently, thereby producing their respective phase voltages [50]-[52]. Also, the implementation of multicarrier PWM schemes is fairly simple as it requires only triangular carrier signals and modulation signals. Furthermore, it can be easily extended to higher output level converters [53]-[55].

On the other hand, the SVM scheme modulates three phases of the converter together, thereby producing the converter line voltages directly. Furthermore, the SVM has flexibility in selecting the switching vectors to fulfil various control objectives such as balancing of DC-bus capacitors and flying capacitors voltage, minimization of common mode voltage, and switching losses reduction [56]-[58]. Also, the SVM improves the DC-bus utilization and exhibits superior steady-state and transient performance compared with the multicarrier PWM schemes [59]-[61]. However, the SVM scheme is difficult to implement for higher output level power converters due to the complex calculations involved in the sector identification, estimation of duty cycles, and the selection of switching vectors [62]-[63]. The multicarrier and SVM schemes are leading in medium and high switching frequency operation of MLIs.

Selective harmonic elimination (SHE) scheme operates at a fundamental switching frequency leading to low switching losses and high efficiency in the MLIs [64]. It requires an offline calculation of switching angles from the non-linear equations, which are designed to eliminate the lower-order harmonics from the converter output voltage/current. This process significantly improves the load power quality. However, the switching angles calculation process becomes tedious as the number of angles increases [65]. Also, the required memory to implement the SHE in the digital control platforms is moderately/notably high. Unlike SVM, SHE exhibits poor transient response, and the implementation complexity increases with the number of control objectives [66], [67].

In this thesis, a five-level MLI is introduced for high-power applications. The new inverter does not require any isolated DC sources and a corresponding phase-shift transformer. The new inverter has a common DC-bus structure, thereby the inverter does not require a DC-bus neutral-point voltage (NPV) controller. Also, it employs fewer flying capacitors and just requires a simple control mechanism to regulate their voltage using multicarrier pulse width modulation (PWM) scheme. However, the flying capacitor voltage controllability varies with the load power factor. This issue is further investigated with different multicarrier PWM schemes. Lastly, a suitable PWM scheme is proposed to handle the new inverter operation for a wide range of load power factors.

2.4 SUMMARY:

Despite the fact that the aforementioned converters have been employed in a variety of applications, they each have their own shortfalls. For example, while some converters, such as the CHB and MMC, offer a modular structure and fault tolerant operation, they still require phase shifting transformers to provide isolated DC sources, increasing the system cost. In the case of MMC, they have a large number of components that limit system reliability. HNPC and SCMC converters require phase shifting transformers as well as clamping diodes, which adds to the complexity. Other converter types, such as NPC, SMC, ANPC, and HC converters, do not require isolated DC sources, but again NPC converters have a large number of clamping diodes. Some converters, such as SMC, ANPC, and HC, do not have clamping diodes and should control both neutral point voltages and FCs. While converters such as FC, MMC, NDC, and NNPC manage only the FCs, they have a large number of components or flying capacitors, which reduces system reliability. Overall, the most commonly used converters have a variety of downsides in the system. As a result, a converter must be designed with the objective of reducing the impact of these downsides on the system.

CHAPTER 3

VOLTAGE BALANCING OF A FIVE-LEVEL MLI

Multilevel inverters (MLIs) can generate output voltage and current waveforms with low harmonic distortion compared with two-level inverters, thereby the output filters can be eliminated. MLIs can also handle low switching frequency operation, leading to low switching losses and improved efficiency [2]-[5]. In addition, the MLIs can handle the medium-voltage (MV) operation using low-voltage semiconductor devices. Therefore, the use of MLIs has become a common practice in various industrial applications, including wind energy, electric drive, power transmission systems, and power quality improvement [2]-[5], [8], [9].

In this chapter, a new five-level MLI is introduced for MV applications. The new inverter is designed with flying capacitors and switching devices only to handle the five-level operation. These flying capacitors should be pre-charged to their nominal value during the start-up process and maintained at the same value throughout normal operation. The charging and discharging processes of the flying capacitors are analyzed with the charge-balance principle and then developed a balancing method to control the flying capacitor's voltage. The performance of the capacitor voltage balancing method is analysed with the conventional phase-disposition pulse width modulation (PD-PWM) scheme. The simulation studies are presented to verify the proposed methodology's performance under steady-state and transient conditions.

3.1 TOPOLOGY AND OPERATION OF A FIVE-LEVEL MLI:

The circuit configuration of the five-level MLI and its operation are presented in the following subsections. Also, a detailed comparison of various five-level MLIs in terms of component count and control complexity is described.

3.1.1 Converter Configuration:

Fig. 3.1 illustrates the three-phase circuit configuration of a new five-level MLI. This inverter is designed with either ten IGBT devices of $v_{dc}/4$ rating or a combination of

six IGBT devices (S_{x1}-S_{x6}) of $v_{dc}/4$ and two devices (S_{x7}-S_{x8}) of $v_{dc}/2$ rating. In addition, each phase needs three flying capacitors (C_{x1}-C_{x3}) of $v_{dc}/4$ rating to achieve a five-level operation, where $x \in \{a, b, c\}$ is the inverter terminal. The inverter does not require any clamping diodes compared with the existing five-level MLIs. Also, the new inverter does not require a DC-bus neutral-point voltage controller and isolated DC sources due to the presence of a single DC-bus structure. The required DC voltage v_{dc} is generated directly by using a rectifier system.

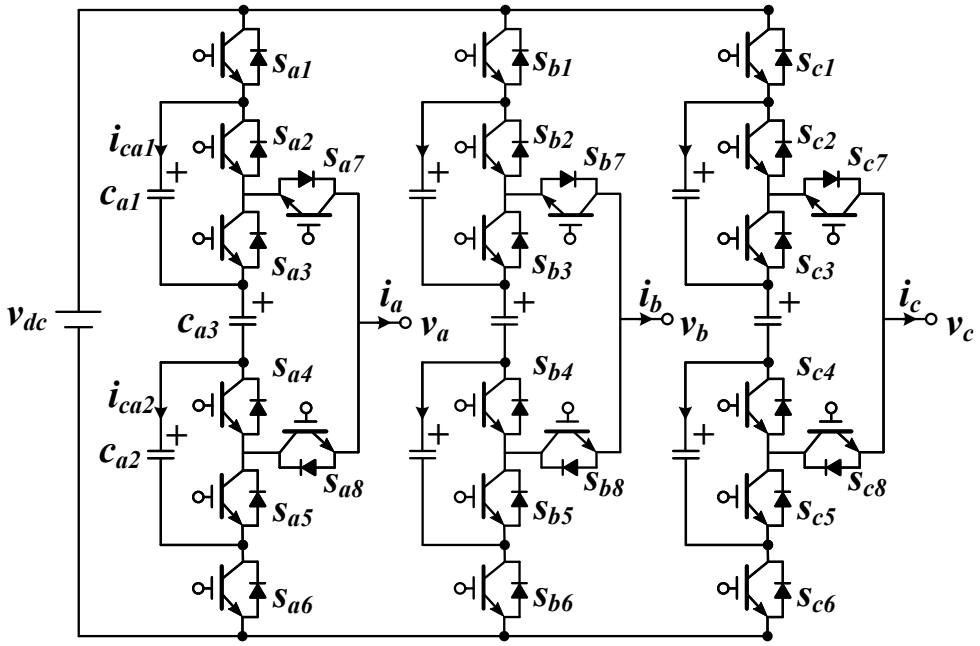


Fig. 3.1: Circuit configuration of the five-level MLI.

3.1.2 Switching States:

The five-level MLI consists of eight switching states per phase as shown in Table 3.1. In this inverter, each flying capacitor voltage should be regulated at $v_{dc}/4$ to generate a five-level voltage waveform at the AC output (v_{xN}), where N is the DC-bus negative terminal. Thus, the eight switching states generate five voltage levels of 0, $v_{dc}/4$, $v_{dc}/2$, $3v_{dc}/4$, and v_{dc} corresponding to their normalized voltage levels (S_x) of **0, 1, 2, 3**, and **4**, respectively. The output voltage (v_{xN}) is defined in terms of normalized voltage level as follows:

$$v_{xN} = S_x \frac{v_{dc}}{4} \tag{3.1}$$

Table 3.1: Switching states of the five-level MLI

S_x	State	v_{xN}	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	$i_x \leq 0$	$i_x > 0$
0	**A1**	*0*	0	0	0	0	1	1	0	1	$v_{cx1} \approx v_{cx2} \approx v_{cx3} \approx$	$v_{cx1} \approx v_{cx2} \approx v_{cx3} \approx$
1	**A2**	$v_{dc}/4$	0	0	0	1	0	1	0	1	$v_{cx1} \approx v_{cx2} \approx v_{cx3} \uparrow$	$v_{cx1} \approx v_{cx2} \approx v_{cx3} \downarrow$
	A3		1	0	0	0	1	0	0	1	$v_{cx1} \downarrow v_{cx2} \downarrow v_{cx3} \downarrow$	$v_{cx1} \uparrow v_{cx2} \uparrow v_{cx3} \uparrow$
2	**A4**	$v_{dc}/2$	0	0	1	0	0	1	1	0	$v_{cx1} \approx v_{cx2} \uparrow v_{cx3} \uparrow$	$v_{cx1} \approx v_{cx2} \downarrow v_{cx3} \downarrow$
	A5		1	0	0	1	0	0	0	1	$v_{cx1} \downarrow v_{cx2} \downarrow v_{cx3} \approx$	$v_{cx1} \uparrow v_{cx2} \uparrow v_{cx3} \approx$
3	**A6**	$3v_{dc}/4$	0	1	0	0	0	1	1	0	$v_{cx1} \uparrow v_{cx2} \uparrow v_{cx3} \uparrow$	$v_{cx1} \downarrow v_{cx2} \downarrow v_{cx3} \downarrow$
	A7		1	0	1	0	0	0	1	0	$v_{cx1} \downarrow v_{cx2} \approx v_{cx3} \approx$	$v_{cx1} \uparrow v_{cx2} \approx v_{cx3} \approx$
4	**A8**	v_{dc}	1	1	0	0	0	0	1	0	$v_{cx1} \approx v_{cx2} \approx v_{cx3} \approx$	$v_{cx1} \approx v_{cx2} \approx v_{cx3} \approx$

$\approx$ - no change, $\uparrow$- charge, $\downarrow$- discharge

From Table 3.1, it is observed that levels **0** and **4** do not have any redundancy states, whereas levels **1**, **2**, and **3** have two states each. The redundancy states **A2** and **A3** generate the same voltage of $v_{dc}/4$ with different turn ON and OFF switches. Similarly, the states **A4** and **A5** generate the same voltage of $v_{dc}/2$, whereas the states **A6** and **A7** generate the same voltage of $3v_{dc}/4$ as shown in Table 3.1. The redundancy states are used to control the flying capacitor's voltage in the new five-level MLI.

3.1.3 Flying Capacitor's Voltage Variation:

Table 3.1 shows the charging and discharging process of the flying capacitor's voltage (v_{cx1}, v_{cx2}, and v_{cx3}) with the current direction for each switching state, respectively. The impact of these switching states on the flying capacitor's voltage is illustrated in Figs. 3.2 and 3.3. The states **A1** and **A8** corresponding to the level **0** and **4** do not affect the voltage of the flying capacitors irrespective of the current direction as shown in Fig. 3.2. On the other hand, the voltage levels **1**, **2**, and **3** have two states each to generate the same voltage level. The states **A2** and **A3** corresponding to level **1** generate the same voltage of $v_{dc}/4$. However, the state **A2** has a charging effect on the capacitor-C_{x3} voltage (v_{cx3}), whereas there is no change in the capacitors C_{x1} and C_{x2} voltages (v_{cx1}

and v_{cx2}) for the negative current direction as shown in Fig. 3.3. On the other hand, the state **A3** has discharging effect on all three flying capacitors voltage for the negative current direction as shown Fig. 3.3. Similarly, the variation of flying capacitor's voltage for other states is described in Table 3.1.

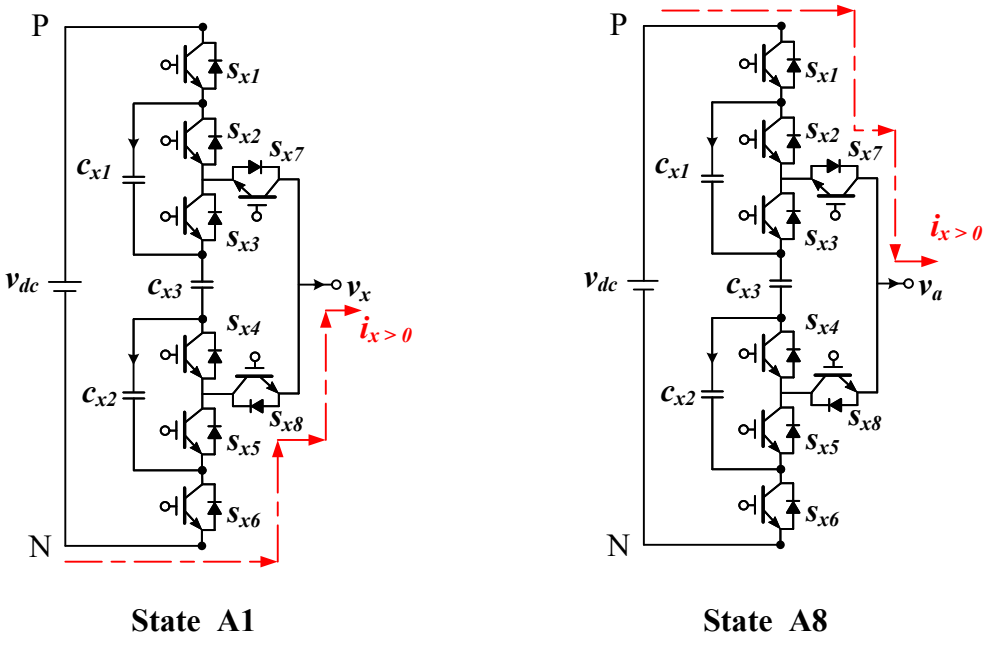


Fig. 3.2: Flying capacitor's voltage variation for states A1 and A8.

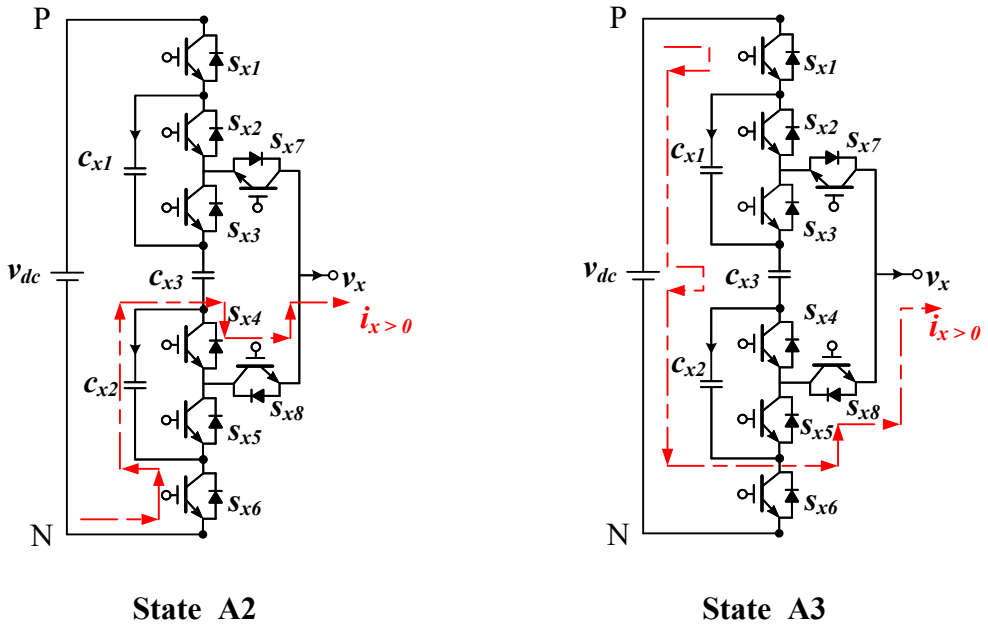


Fig. 3.3: Flying capacitor's voltage variation for states A2 and A3.

3.1.4 Comparison of Five-Level MLIs:

Over the years, several five-level MLIs have been developed for high-power applications. A brief comparison of these five-level MLI topologies in terms of component count and control complexity is summarized in Table. 3.2 and 3.3. In this comparison, the active devices, clamping diodes, and flying capacitors (FCs) with an identical voltage rating of $v_{dc}/4$ are considered. Among them, the cascaded H-bridge (CHB), H-bridge neutral-point clamped (HNPC), and series-connected multilevel converter (SCMC) topologies require more DC sources with isolated structure as shown in Table 3.2 [68]-[71]. To generate the isolated DC sources, these topologies require a phase-shift transformer with multiple secondary windings, which leads to an increase in the overall system cost and size [68]-[71]. However, these topologies have high reliability due to their modular structure and are suitable for fault-tolerant operation.

Table 3.2: Comparison of the five-level MLIs (part-1)

Characteristics	CHB	HNPC	SCMC	NPC	SMC	ANPC	HC	NNPP
Active Switches	24	24	24	24	36	36	30	36
Clamping Diodes	-	12	12	36	-	-	-	-
Flying Capacitors	-	-	-	-	6	3	9	6
Number of DC Sources	6	3	3	1	1	1	1	1
Isolated DC Sources	Yes	Yes	Yes	No	No	No	No	No
DC-Bus NPV Control	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
FCs Voltage Control	No	No	No	No	Yes	Yes	Yes	Yes

On the other hand, the five-level MLIs without isolated DC sources are also introduced in the literature [72]-[77]. These inverters require a single DC source and can eliminate the need for a phase-shift transformer. Therefore, these topologies are cost-effective compared with CHB, HNPC, and SCMC topologies, but they have less reliability due to the lack of modular construction. Among them, the neutral-point clamped (NPC) converter uses clamping diodes along with split DC-bus philosophy to achieve multilevel operation. This topology requires more clamping diodes and a complex control mechanism to regulate the multiple DC-bus neutral-points voltage

(NPV). Due to the presence of more components, the manufacturing and assembling process of the NPC is quite challenging [72]-[77]. Hence, the NPC is not often used for five-level operations. Alternatively, the flying capacitors together with split DC-bus philosophy are adopted in the stacked multicell (SMC), active neutral-point clamped (ANPC), hybrid converter (HC), and nested neutral-pilot point (NNPP) converters to handle the five-level operation as shown in Table 3.2 [72]-[77]. This approach eliminates the clamping diodes and reduces the number of DC-bus neutral points compared with the NPC. However, these topologies still require both DC-bus NPV and flying capacitors (FCs) voltage control mechanisms, which leads to increased overall system control complexity.

Table 3.3: Comparison of the five-level MLIs (part-2)

Characteristics	FC	MMC	NDC	NNPC	New 5L-MLI
Active Switches	24	48	24	24	30
Clamping Diodes	-	-	18	6	-
Flying Capacitors	18	24	9	15	9
Number of DC Sources	1	1	1	1	1
Isolated DC Sources	No	No	No	No	No
DC-Bus NPV Control	No	No	No	No	No
FCs Voltage Control	Yes	Yes	Yes	Yes	Yes

On the other hand, the flying capacitor (FC) converter, modular multilevel converter (MMC), nested diode-clamped (NDC), and nested neutral-point clamped (NNPC) topologies are designed without split DC-bus philosophy, thereby the DC-bus NPV controller can be eliminated as shown in Table 3.3 [72]-[77]. Also, these topologies require either more flying capacitors or clamping diodes to handle the five-level operation, which leads to a significant rise in the total component count. Also, the use of more flying capacitors increases the complexity of the flying capacitor voltage control mechanism and affects the inverter reliability [72]-77].

Compared with the existing MLIs, the new inverter does not require clamping diodes and has a low total component count. Also, it does not require isolated DC sources and the corresponding phase-shift transformer. The new inverter does not require a DC-

bus NPV voltage controller due to the absence of the split DC-bus structure. Furthermore, the inverter uses a smaller number of flying capacitors and requires their voltage control mechanism only. Hence, the overall control complexity of the new inverter is relatively low compared with the existing inverters.

Table 3.4: Flying capacitor neutral-point currents

State	v_{xo}	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	i_{xN1}	i_{xN2}
A1	$-v_{dc}/2$	0	0	0	0	1	1	0	1	**0**	**0**
A2	-	0	0	0	1	0	1	0	1	**0**	i_x
A3	$v_{dc}/4$	1	0	0	0	1	0	0	1	**0**	**0**
A4	*0*	0	0	1	0	0	1	1	0	i_x	**0**
A5		1	0	0	1	0	0	0	1	**0**	i_x
A6	$v_{dc}/4$	0	1	0	0	0	1	1	0	**0**	**0**
A7		1	0	1	0	0	0	1	0	i_x	**0**
A8	$v_{dc}/2$	1	1	0	0	0	0	1	0	**0**	**0**

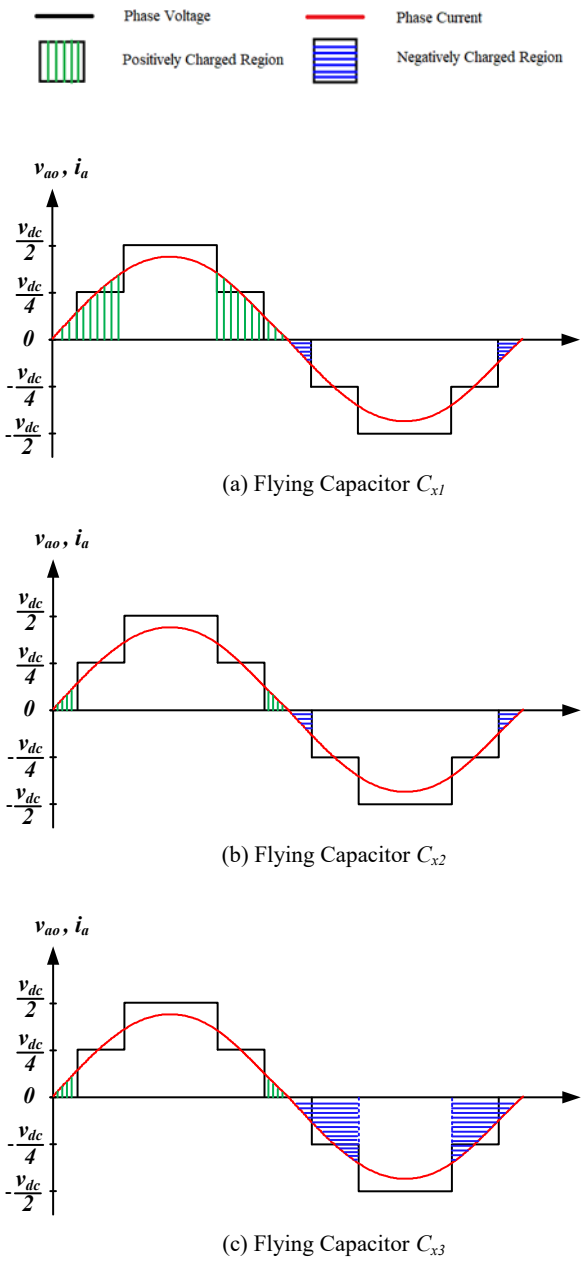
3.2 ANALYSIS AND MODELLING OF FLYING CAPACITOR'S VOLTAGE:

In this subsection, the natural balancing of the flying capacitor's voltage in the new five-level inverter is analysed with the charge-balance principle. According to the charge-balance principle, the average charge stored in each flying capacitor for one fundamental cycle (60 Hz frequency) should be zero to achieve a natural balancing of the flying capacitor's voltage.

3.2.1 Analysis of Flying Capacitor's Voltage:

The analysis is conducted at the unity power factor ($\varphi = 0^o$, where φ is the power factor angle) and zero power factor ($\varphi = 90^o$) and the corresponding theoretical analysis are shown in Figs. 3.4 and 3.5, respectively. According to the states given in Table 3.1, the states **A1** and **A8** entirely bypass the three flying capacitors and do not cause any unbalance in the flying capacitor's charge. On the other hand, the states **A3** and **A6** result in a series connection of all three flying capacitors and have an identical effect on them. Therefore, these states also do not have any unbalance effect on the flying capacitor's charge. The rest of the states **A2**, **A4**, **A5**, and **A7** have an unbalanced effect on the flying

capacitor's charge due to the current flow through the flying capacitor's neutral points (N_{x1} and N_{x2}). These currents are given for each switching state in Table 3.4.



(a) Flying Capacitor C_{x1}

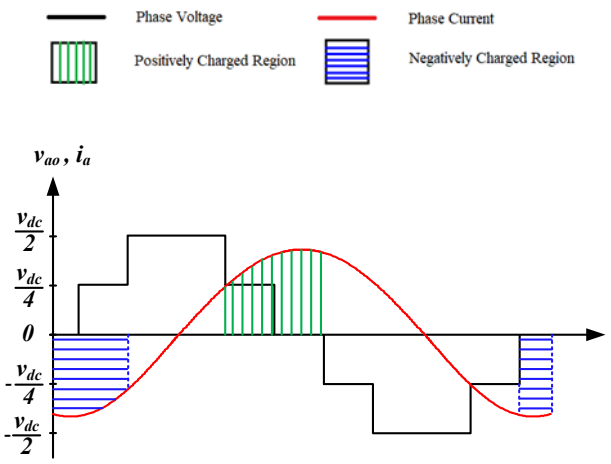
(b) Flying Capacitor C_{x2}

(c) Flying Capacitor C_{x3}

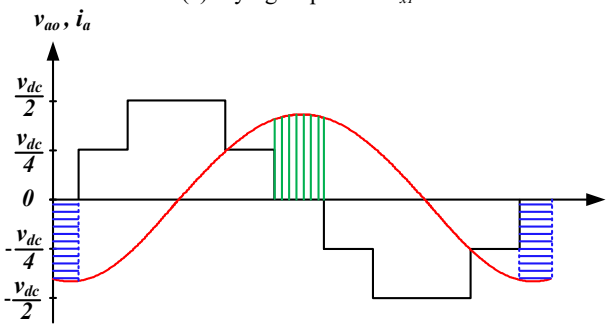
Fig. 3.4: Flying capacitors charge balance analysis at the unity power factor.

From the charge-balance principle, it is observed that the flying capacitor C_{x1} and C_{x3} have a positive and negative average charge for one fundamental cycle under unity power factor operation as shown in Fig. 3.4. Therefore, the flying capacitor C_{x1} and C_{x3} voltages continuously increase and decrease, respectively, if they are not controlled properly. On the other hand, the flying capacitor C_{x2} has zero average charges for one

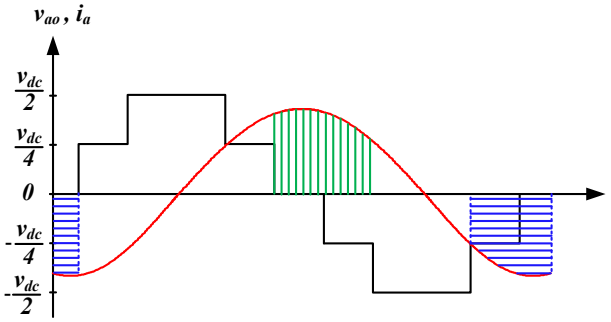
fundamental cycle, which leads to the natural balancing of its voltage. Similarly, the analysis at zero power factor conducted and corresponding results are shown in Fig. 3.5. Under this condition, the flying capacitor C_{x1}, C_{x2}, and C_{x3} have zero average charges for one fundamental cycle, which leads to natural balancing of their voltages. It is also noted that the flying capacitor voltage balancing depends on the active power rather than the reactive power supplied by the inverter. Even though the natural balancing of the flying capacitor's voltage is achievable with the switching states given in Table 3.4, for safety issues it is necessary to have a voltage control mechanism.



(a) Flying Capacitor C_{x1}



(b) Flying Capacitor C_{x2}



(c) Flying Capacitor C_{x3}

Fig. 3.5: Flying capacitors charge balance analysis at zero power factor (lag).

3.2.2 Modelling of Flying Capacitor's Voltage:

The flying capacitor voltages are further analyzed mathematically. Considering the switching states given in Table 3.4, the equivalent representation of the flying capacitor neutral-point currents (i_{Nx1} and i_{Nx2}) is shown in Fig. 3.6. In this analysis, the flying capacitors with identical capacitance ($C_{x1} = C_{x2} = C_{x3} = C$) are considered in order to reduce the maintenance cost of the system. The impact of the average neutral point currents (I_{Nx1} and I_{Nx2}) on each flying capacitor voltage for one switching period (T_s) is given as follows:

$$\left.\begin{aligned} \Delta v_{cx1} &= \left(\frac{2}{3}\, I_{Nx1} + \frac{1}{3}\, I_{Nx2}\right) \frac{T_S}{C} \\ \Delta v_{cx2} &= (\, I_{Nx2} - \, I_{Nx1}) \, \frac{T_S}{C} \\ \Delta v_{cx3} &= \left(-\frac{1}{3}\, I_{Nx1} - \frac{2}{3}\, I_{Nx2}\right) \frac{T_S}{C} \end{aligned}\right\} \tag{3.2}$$

The unbalanced voltage of the flying capacitors C_{x1} and C_{x3} is given as

$$\Delta v_{cx1} - \Delta v_{cx3} = (\, I_{Nx1} + \, I_{Nx2}) \, \frac{T_S}{C} \tag{3.3}$$

From equations (3.2) and (3.3), it is observed that the flying capacitors C_{x1}, C_{x2}, and C_{x3} voltages can be balanced provided that the average neutral-point currents I_{Nx1} and I_{Nx2} should be equal and opposite in-phase.

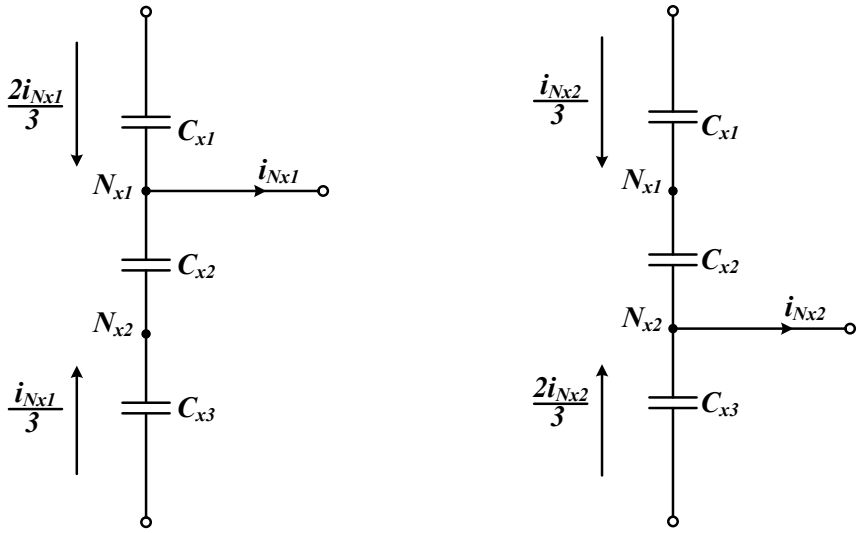


Fig. 3.6: Flying capacitor's neutral point currents.

The flying capacitor neutral-point currents are expressed as follows:

$$\left.\begin{aligned} i_{Nx1} &= S_{x7}(1 - S_{x2})\, i_x \\ i_{Nx2} &= S_{x8}\,(1 - S_{x5})\, i_x \end{aligned}\right\} \tag{3.4}$$

From equation (3.4), it is observed that the flying capacitor neutral-point currents can be controlled by adjusting the duty cycles of the switching devices S_{x2}, S_{x5}, S_{x7}, and S_{x8}. The switching device's duty cycles can be adjusted through the well-designed pulse width modulator, which is the focus of this work. In this study, the carrier-based pulse width modulator is used to adjust the switching device's duty cycles. The duty cycle adjustment can be accomplished by modifying either modulation signals or triangular carrier signals. However, the modification of triangular carrier signals can be easily achieved and is considered in the present study. This research work is focused on the capacitor voltage balancing performance with different triangular carrier signal arrangements.

3.3 MODULATION AND VOLTAGE BALANCING METHOD:

Multicarrier pulse width modulation (PWM) schemes are easy to implement for five-level MLIs compared with the space vector modulation scheme. It also has good dynamic performance compared with the selective harmonic elimination (SHE) scheme [55], [59], [66]. In the multi-carrier PWM method, the triangular carrier signals are arranged across the carrier space and compared with the reference signal. If the carrier signals are disposed of vertically, then it is referred to as level-shifted carrier PWM (LSC-PWM) and if the carrier signals are disposed of horizontally, then the resultant method is referred to as phase-shifted carrier PWM (PSC-PWM) [50]-[55]. These PWM schemes are considered in the present study to investigate the voltage balancing issues in the five-level inverter.

3.3.1 Level-Shifted Carrier PWM Schemes:

The LSC-PWM has three different variations, and they are named phase-disposition PWM (PD-PWM), phase-opposition disposition PWM (POD-PWM), and alternate phase-opposition disposition PWM (APOD-PWM) schemes. The carrier arrangement of these schemes is shown in Fig. 3.7. To implement these schemes for a five-level inverter, a total of four triangular carrier signals (C_1-C_4) are required. In PD-

PWM all the carriers are in the same phase; in POD-PWM the carriers below zero references are 180º out of phase with the carriers above zero reference, and in APOD the alternative carriers are in the opposite phase with each other. Among them, the PD-PWM scheme has superior harmonic performance compared with the POD-PWM and APOD-PWM schemes [52]. Hence, the PD-PWM is considered in the present study.

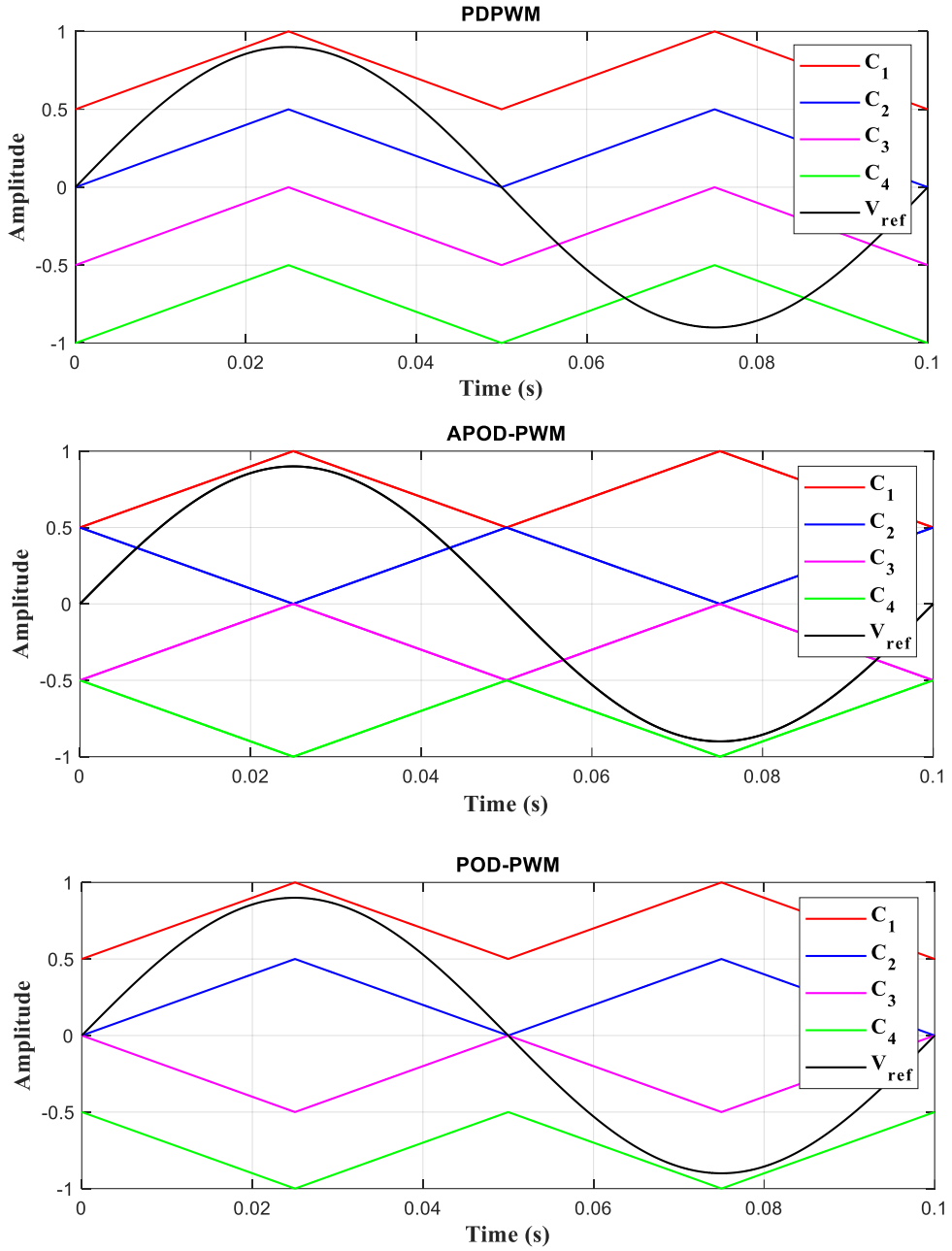


Fig. 3.7: Carrier arrangement of LSC-PWM schemes.

The triangular carrier and modulation signals arrangement in the PD-PWM is shown in Fig. 3.7. All the carrier signals are generated with an amplitude of V_{cr} and the carrier frequency of f_{cr}. The reference modulation signals (v^*_x) are generated with the required amplitude modulation index of m_a, the output frequency f_o, and an initial phase angle $\theta_x \in (0, \frac{2\Pi}{3}, \frac{4\Pi}{3})$. It is mathematically expressed as follows:

$$v_x^* = m_a \sin(2\pi f_o t + \theta_x) \tag{3.5}$$

Each triangular carrier signal is compared with the modulation signal, and the resultant output of each comparison is combined to form a normalized voltage level waveform (S_x) as shown in Fig. 3.8. The normalized voltage waveform has voltage levels of **0**, **1**, **2**, **3**, and **4**. These voltage levels are fed to the redundancy switching states selection method to balance the flying capacitor's voltage.

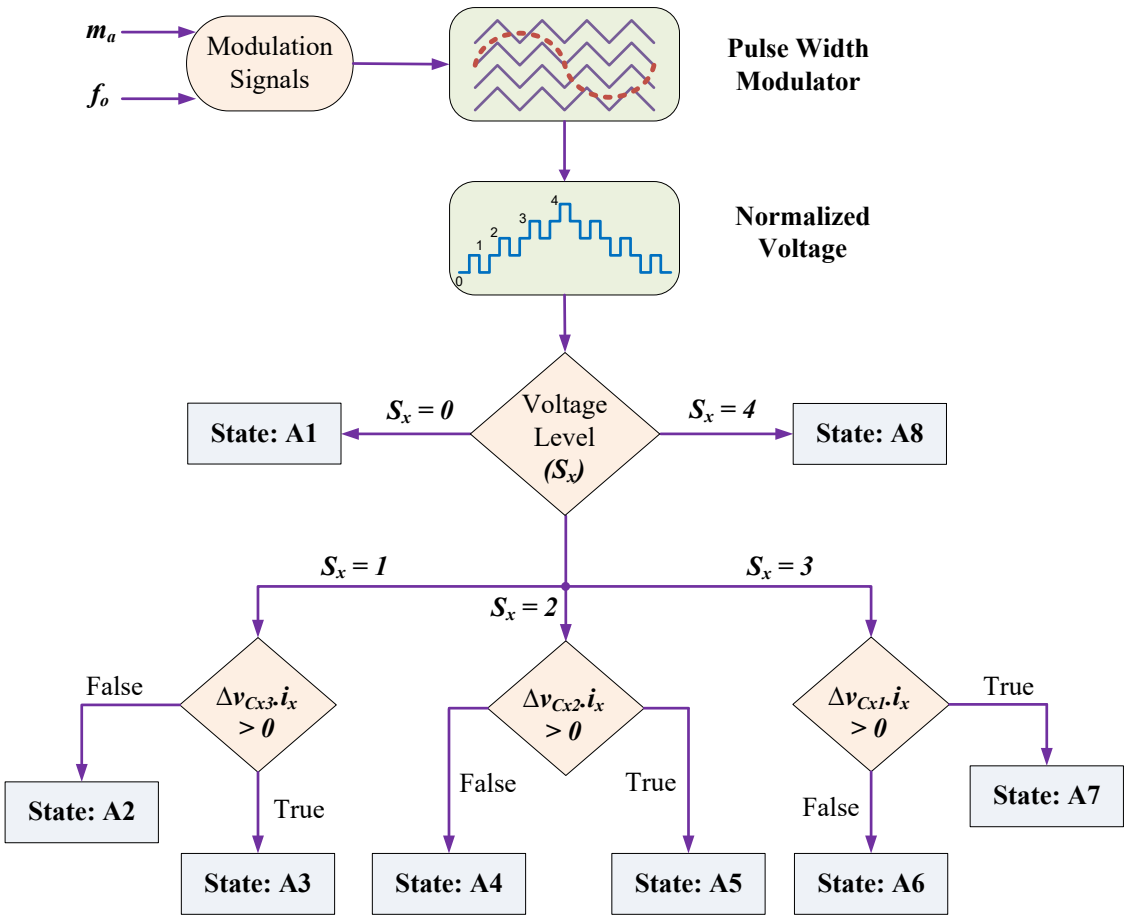


Fig. 3.8: Voltage Balancing Method using PD-PWM scheme.

3.3.2 Voltage Balancing Method:

The switching states selection process with the normalized voltage level in the five-level inverter is illustrated in Fig. 3.8. From the comparison of reference and triangular carrier signals, the normalized voltage levels (S_x) are generated. From Table 3.5, states **A1** and **A8**, and their respective device switching states are directly selected when $\boldsymbol{S_x = 0}$ and $\boldsymbol{S_x = 4}$, respectively. These states do not have any redundancy, and hence there is no selection criterion for them. When $\boldsymbol{S_x = 1}$, $\boldsymbol{S_x = 2}$, and $\boldsymbol{S_x = 3}$, then there is a need for selection criteria as they have multiple states such as **A2/A3**, **A4/A5**, and **A6/A7**, respectively. This selection criterion is designed based on the deviation of flying capacitor voltage and current direction (i_x). The deviation of flying capacitor voltage is calculated as follows:

$$\left.\begin{aligned} \Delta V_{cx1} &= v_{cx1} - \tfrac{V_{dc}}{4} \\ \Delta V_{cx2} &= v_{cx2} - \tfrac{V_{dc}}{4} \\ \Delta V_{cx3} &= v_{cx3} - \tfrac{V_{dc}}{4} \end{aligned}\right\} \tag{3.6}$$

From Table 3.5 analysis, the capacitor C_{x3} is considered during the selection of states **A2/A3**, when the voltage level $\boldsymbol{S_x = 1}$. For example, the $\Delta V_{cx3} > 0$ represents the measured value of the flying capacitor voltage greater than the nominal voltage. In that case, the flying capacitor C_{x3} should be discharged to reach its rated value. To meet this requirement, state **A3** is selected for $i_x > 0$, whereas state **A2** is selected for $i_x \leq 0$. Considering both current direction and flying capacitor voltage deviation, the condition $\Delta V_{cx3} * i_x > 0$ is derived. If this condition is true, then the state **A3** is selected otherwise, the state **A2** is chosen for $\boldsymbol{S_x = 1}$**.** Similarly, the conditions $\Delta V_{cx2} * i_x > 0$ and $\Delta V_{cx1} * i_x > 0$ are derived based on the information given in Table 3.5 to select the states A4/A5 and A6/A7 for $\boldsymbol{S_x = 1}$ and $\boldsymbol{S_x = 3}$, respectively. With the designed criteria, the most appropriate state and respective device switching states are selected and applied to the inverter, which guarantees the perfect regulation of the flying capacitor's voltage.

Table 3.5: Selection Of Redundancy Switching States

S_x	State	$i_x \leq 0$	$i_x > 0$
0	**A1**	-	-
1	**A2**	$\Delta V_{cx3} \geq 0$	$\Delta V_{cx3} < 0$
	A3	$\Delta V_{cx3} < 0$	$\Delta V_{cx3} \geq 0$
2	**A4**	$\Delta V_{cx2} \geq 0$	$\Delta V_{cx2} < 0$
	A5	$\Delta V_{cx2} < 0$	$\Delta V_{cx2} \geq 0$
3	**A6**	$\Delta V_{cx1} \geq 0$	$\Delta V_{cx1} < 0$
	A7	$\Delta V_{cx1} < 0$	$\Delta V_{cx1} \geq 0$
4	**A8**	-	-

3.4 SIMULATION STUDIES:

The simulation studies are conducted on a 5 MVA/4.16 kV rated five-level inverter using MATLAB/Simulink tool. Each flying capacitor is designed with a capacitance of 3000 μF and a rated voltage of 1.5 kV. The value of capacitance is selected based on safe handling of voltage ripple and capacitance availability in the market. The triangular carrier signals are generated with a carrier frequency of 1 kHz. The passive load is constructed with a series connection of resistor and inductor.

3.4.1 Steady-state Performance:

Fig. 3.9 shows the voltage balancing performance with the PD-PWM scheme at a power factor (PF) of 0.55 (lag). The modulation signals are generated with a modulation index of 0.99 and a frequency of 60 Hz. The inverter produces a symmetrical stepped voltage waveform with a step of 1500 V. Also, each switching period causes one voltage step change only. As a result, the voltage has a total harmonic distortion (THD) of 16.15%. The three-phase load currents have less ripple because of the symmetrical stepped voltage waveform, which results in a harmonic distortion of 1.09% as shown in Fig. 3.9(b). These harmonics are calculated using the Fast Fourier Transform toolbox in the MATLAB. The flying capacitor voltages of phase-*a* and phase-*b* are shown in Fig. 3.9(c) and (d), respectively. Even though the flying capacitor voltages are maintained close to their rated value of 1500 V, these capacitors still exhibit uneven voltage ripples. These unequal ripples are mainly due to the unequal neutral-point current (i_{Nx1} and i_{Nx2}) as per the analysis given in subsection 3.2.1.

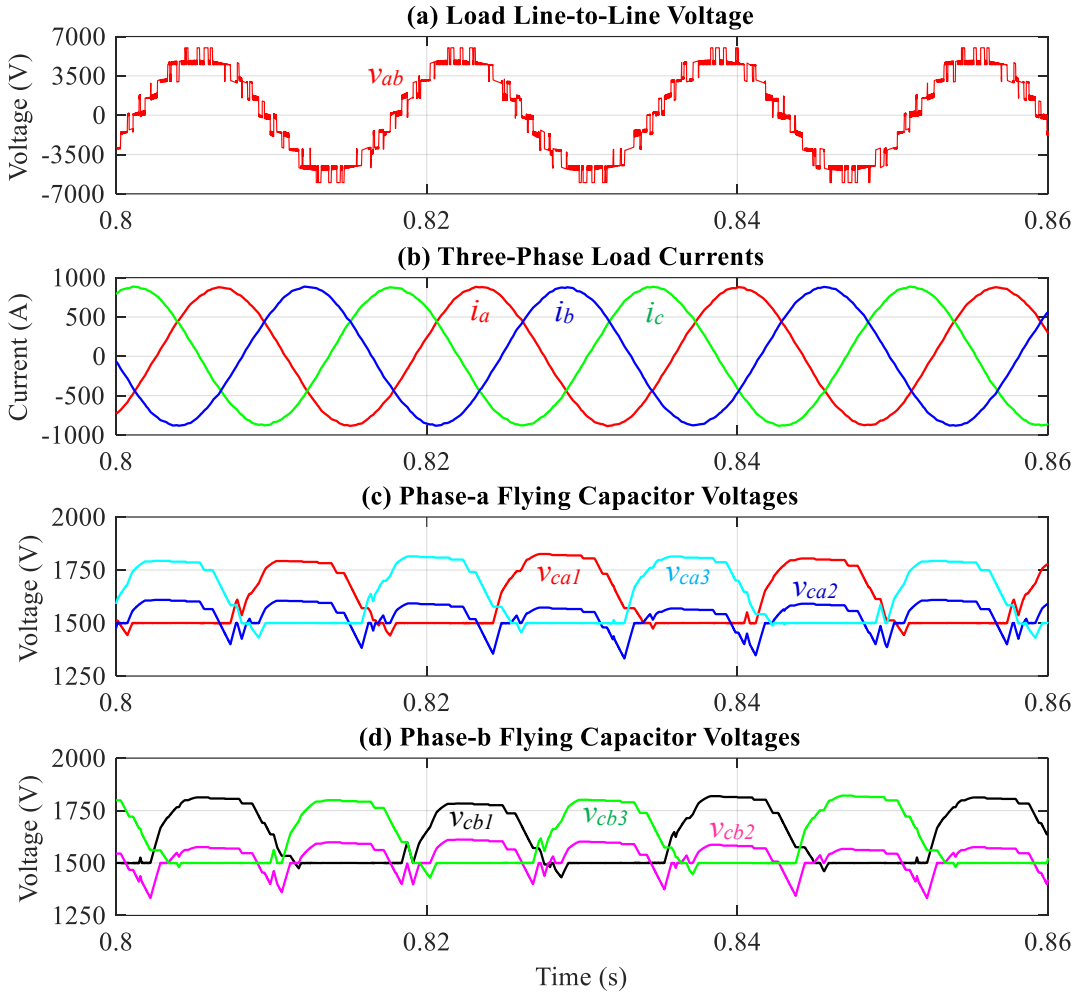


Fig. 3.9: Steady-state performance at a power factor of 0.55 (lag).

Fig.3.10 shows the simulation performance of the voltage balancing method at a load power factor of 0.85 (lag). As the power factor increases, the PD-PWM scheme is unable to maintain the flying capacitor's voltage at its rated voltage as shown in Fig. 3.10. The flying capacitor C_{x2} voltage is deviated from its rated value, whereas the flying capacitor's C_{x1} and C_{x3} voltages are maintained at their rated value of 1500 V. However, the unequal voltages cause non-uniform steps in the output voltage leading to a higher THD of 21.19%. Also, the load currents deviate from their sinusoidal nature and have a THD of 2.71%. The other power factors are analysed and the cut off power factor for capacitor voltage balancing is found to be approximately 0.65 (lag). Hence, the simulation analysis is performed for power factors 0.55 (lag) and 0.85 (lag) in order to make sure that the system does not run under lower efficiency condition (i.e. low power factor) and within safe operating conditions (i.e. not close to unity) to avoid worse case.

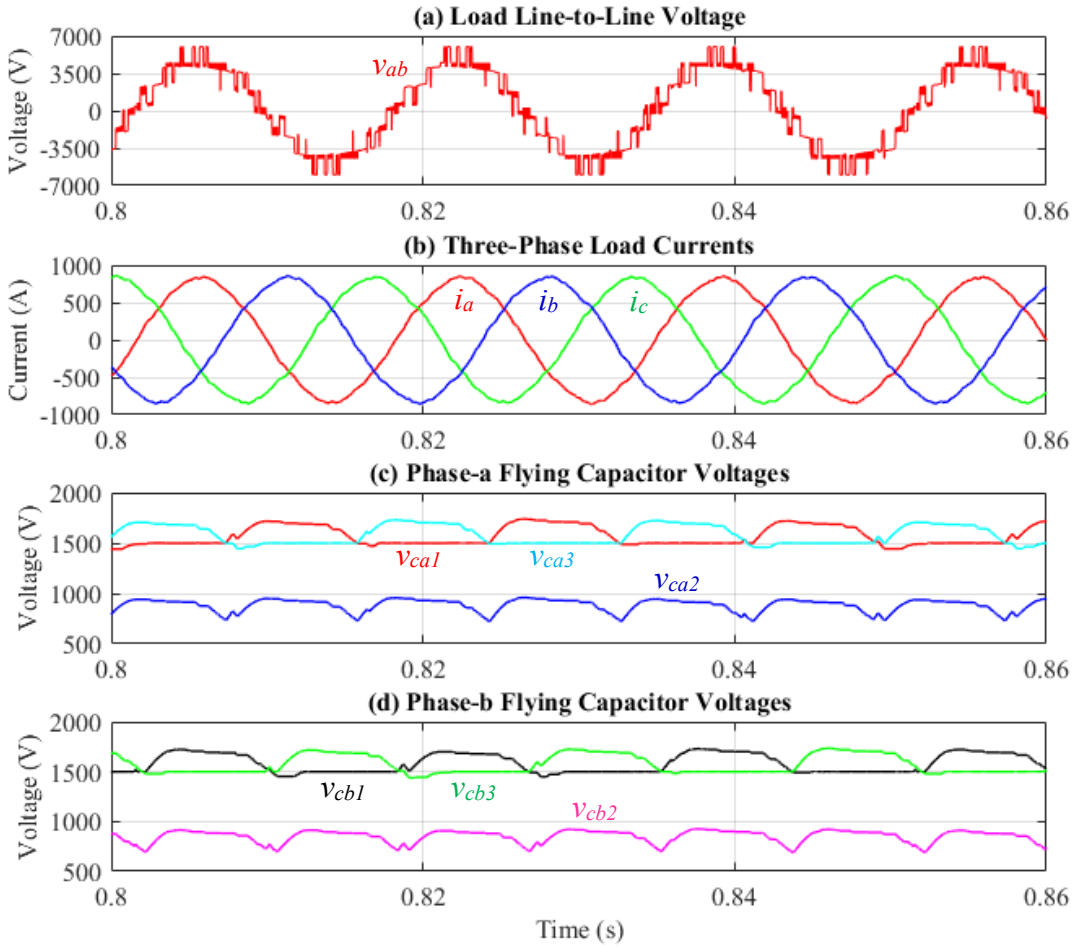


Fig. 3.10: Steady-state performance at a power factor of 0.85 (lag).

3.4.2 Transient Performance:

Fig.3.11 shows the performance of the voltage balancing method under step change in the modulation index. The step change in modulation index from 0.4 to 0.9 is applied at time 0.825 s. In this study, the frequency of the modulation signals is set to 60 Hz. With the increase in the modulation index, the number of steps in the output voltage is increased, leading to a decrease in the harmonic distortion from 40.68% to 16.76% as shown in Fig.3.11(a). Also, the load currents magnitude increased with the modulation index as shown in Fig.3.11(b). These currents have a THD of 1.77% at a modulation index of 0.4, which is reduced to 0.99% at a modulation index of 0.9. The flying capacitor voltages of phase-*a* and phase-*b* are maintained at their rated value of 1500 V as shown in Figs.3.11(c) and (d), respectively. Also, the voltage ripples increased with the modulation index, and they have a ripple of 250 V and 391 V (p-p) at a modulation index of 0.4 and 0.9, respectively.

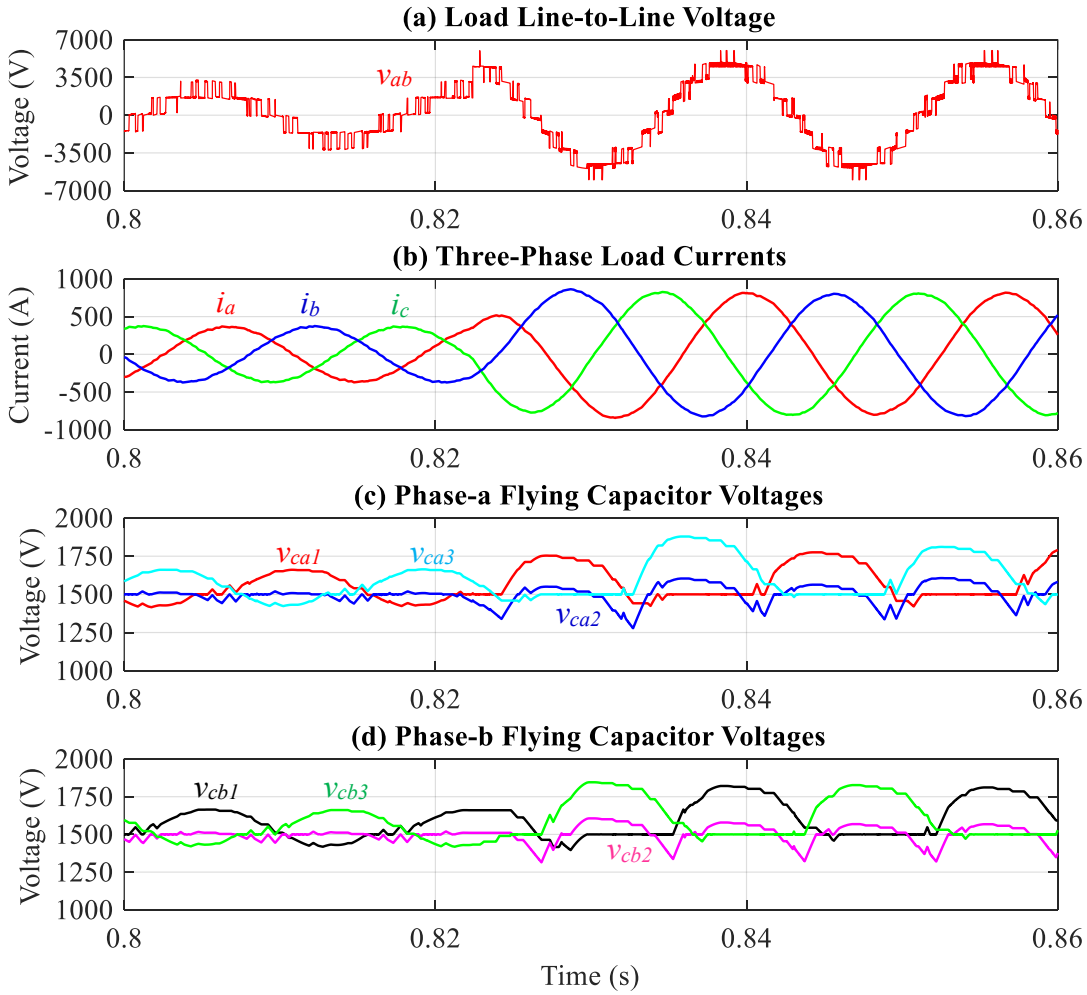


Fig. 3.11: Transient performance analysis.

3.4.3 Performance Analysis:

The performance of the five-level inverter with the PD-PWM is analyzed in terms of voltage harmonic distortion ($\%V_{THD}$), the current harmonic distortion ($\%I_{THD}$), and capacitor voltage ripple at different modulation indices (m_a) in consideration of IEEE-519 standards for harmonics and a tolerable capacitor voltage ripple of around 20%. The voltage harmonic distortion decreases with the increase in m_a due to the rise in the number of steps in the output voltage as shown in Fig.3.12(a). Also, the current harmonic distortion decreases with the m_a as shown in Fig. 3.12(b). On the other hand, the capacitor voltage ripple increases with the rise in modulation index due to the increase in the load current magnitude as shown in Fig. 3.12(c). This is because an increase in modulation index causes an increase in voltage, which resulting an increase in the current magnitude as per Ohm's law. The rate of charge through the capacitor increases as the magnitude of

the current increases, resulting in increasing capacitor voltage ripple. Also, as the modulation index increases, the number of voltage steps increases, making the output waveform more similar to the fundamental, and thus the system's harmonics reduce.

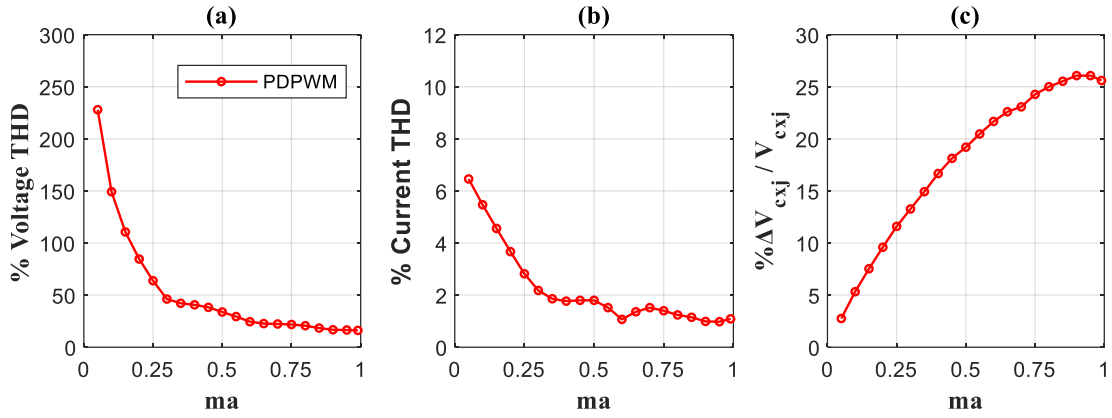


Fig. 3.12: Performance analysis at a power factor of 0.55 (lag): (a) voltage harmonic distortion ($\%V_{THD}$), (b) current harmonic distortion ($\%I_{THD}$), and (c) Flying capacitor voltage ripple ($\%\Delta V_{Cxj}/V_{Cxj}$).

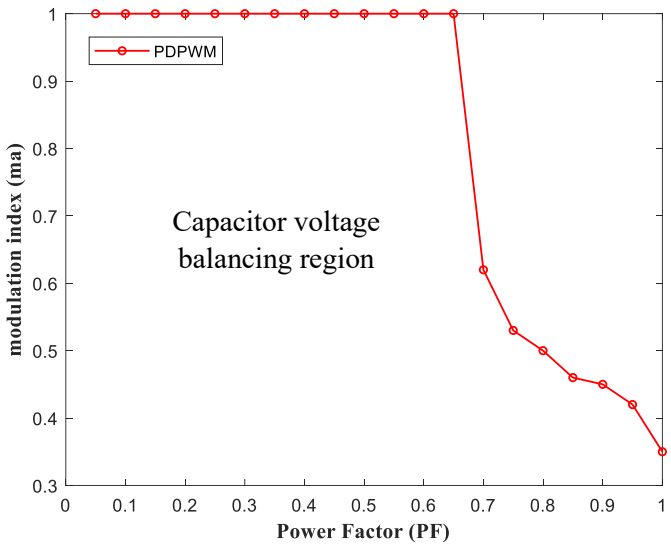


Fig. 3.13: Voltage balancing boundary limits of PD-PWM.

3.4.4 Voltage Balancing Boundary Limits:

Fig. 3.13 depicts the voltage balancing boundary limits of the PD-PWM scheme. These boundary limits are calculated through simulations at various power factors and modulation indices. It is observed that the PD-PWM scheme can balance the capacitor's

voltage up to a load power factor of 0.65 when the modulation index is equal to unity. At higher power factors, the modulation index must decrease to maintain the capacitor's voltage at its rated value. Overall, the voltage balancing in the five-level MLI is difficult to achieve under a wide range of load power factors and modulation indices.

3.5 SUMMARY:

In this chapter, the operation and switching states of the five-level MLI are introduced. The natural balancing of the flying capacitor's voltage is analyzed using the charge-balance principle. Also, the mathematical models for the flying capacitor voltages are presented. To control the flying capacitor's voltage, a simple methodology based on the redundancy switching states is described. The performance of the voltage balancing method with the PD-PWM scheme is verified using the simulation tools. The results show the PD-PWM has good harmonic performance, but it has limited balancing ability and can only maintain the capacitor's voltage at its rated value up to a load power factor of 0.65 at $m_a = 1$, which is the limitation of the PD-PWM scheme.

CHAPTER 4

MODIFIED MULTICARRIER PWM SCHEMES FOR FIVE-LEVEL MLI

The studies in Chapter 3 show that the PD-PWM scheme has superior harmonic performance and can meet the IEEE-519 harmonic standards [78], [79]. However, this scheme is unable to balance the flying capacitor's voltage in the five-level MLI under a wide range of load power factors and modulation indices. To address this issue, the modified multicarrier PWM schemes are investigated in this chapter.

In this chapter, the modified multicarrier PWM schemes including phase-shifted carrier PWM (PSC-PWM) and modified PD-PWM are introduced for the five-level MLI. The modified PD-PWM is also referred to as carrier-overlap PWM (COPWM) in this study. Additionally, the principle and implementation of these schemes are presented. The steady-state and transient performance analysis under different load power factors is conducted using MATLAB simulation tools. Finally, a brief comparison of PD-PWM, PSC-PWM, and COPWM schemes is provided.

4.1 PHASE-SHIFT CARRIER PWM SCHEME:

In the PD-PWM scheme, the triangular carrier signals are disposed of vertically in the carrier space with the same magnitude and zero phase shift. On the other hand, the triangular carrier signals are disposed of horizontally in the phase-shift carrier PWM (PSC-PWM) scheme as shown in Fig. 4.1. These carriers have the same magnitude of V_{cr}, frequency of f_{cr}, and a phase shift of 90° (360/4 = 90°). The reference modulation signals (v^*_x) are generated with the required amplitude modulation index of m_a, the output frequency of f_o, and an initial phase angle of $\theta_x \epsilon (0, \frac{2\Pi}{3}, \frac{4\Pi}{3})$. Each triangular carrier signal is compared with the modulation signals, and their comparison outputs are added together. The resultant output is equivalent to the normalized output voltage waveform. This information is used together with the voltage balancing method shown in Fig. 3.8 to select the appropriate redundancy switching state to regulate each flying capacitor voltage at its rated value.

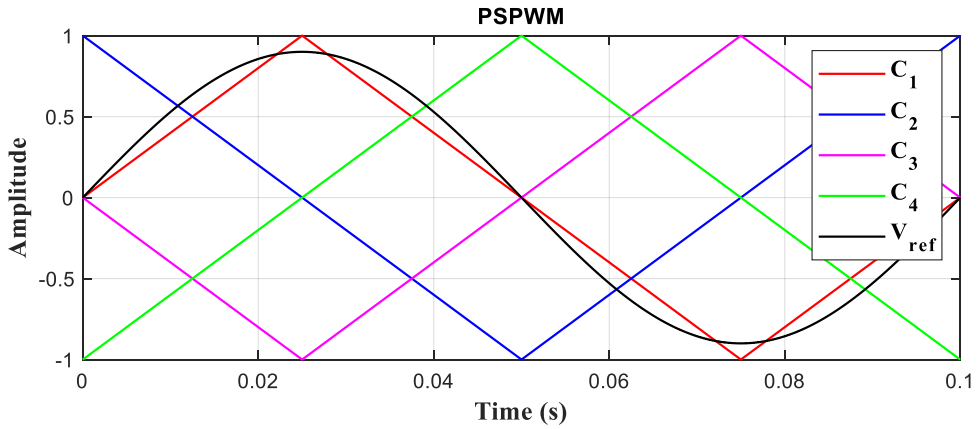


Fig. 4.1: Carrier arrangement in the PSC-PWM scheme.

4.2 SIMULATION STUDIES:

The simulation studies are conducted on a 5 MVA/4.16 kV capacity five-level MLI. Each flying capacitor is designed with a capacitance of 3000 μF and a rated voltage of 1.5 kV. The carrier signals of PSC-PWM are generated with a frequency of 250 Hz so that the inverter equivalent switching frequency is equal to 1000 Hz. By doing so, the PD-PWM and PSC-PWM schemes result in identical switching frequencies of MLI.

4.2.1 Steady-state Performance:

The steady-state performance of the voltage balancing method with PSC-PWM is shown in Fig. 4.2. In this study, the modulation signals are generated with a modulation index of 0.99 and a frequency of 60 Hz. The load power factor is maintained at 0.55 (lag). The inverter produces an output voltage with a total harmonic distortion of 23.05%, which is higher than the PD-PWM performance as shown in Fig. 4.2(a). The uneven switching actions lead to higher ripple and THD in the output current, which is around 1.66% as shown in Fig. 4.2(b). This THD is 52% higher when compared to the current harmonics in PD-PWM. The flying capacitor voltages of phase-*a* and phase-*b* are maintained close to their rated values of 1500 V as shown in Figs. 4.2(c) and 4.2(d), respectively. However, the charging and discharging processes of flying capacitors are not uniform leading to different voltage ripples as shown in Fig. 4.2. This also shows that the voltage ripple in the capacitors with PSC-PWM is 7% higher than for PD-PWM, making the system more unstable.

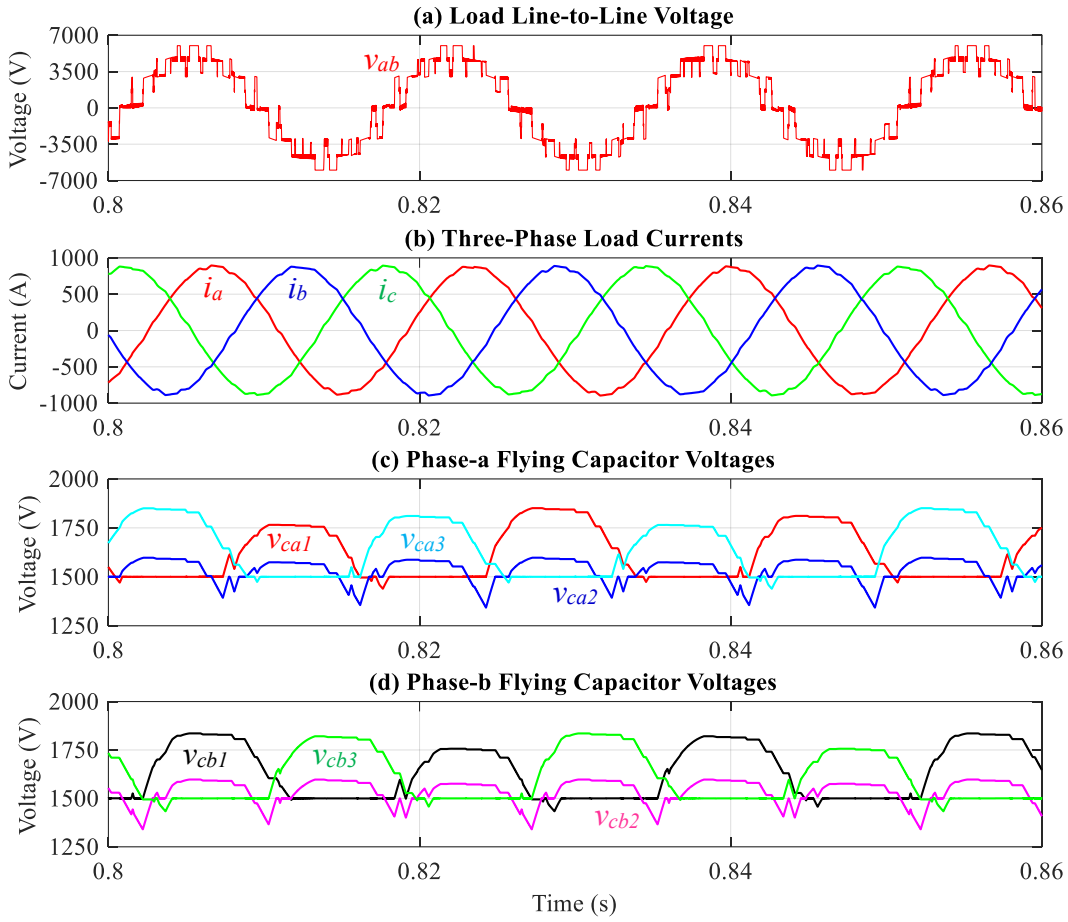


Fig. 4.2: Steady-state performance at a power factor of 0.55 (lag).

The performance of the voltage balancing method with the PSC-PWM scheme at a load power factor of 0.85 (lag) is shown in Fig. 4.3. In this study, the modulation signals are generated with a modulation index of 0.99 and a frequency of 60 Hz. It is observed that the charge balance is unable to achieve with the PSC-PWM at higher power factors. Therefore, the flying capacitors C_{x1} and C_{x3} are maintained at their rated values of 1500 V, whereas the flying capacitor C_{x2} voltage deviated from its rated value. The unbalance in the flying capacitor's voltage led to higher THD in the output voltage and current waveforms of 27.68% and 3.55%, respectively. In comparison with PD-PWM, the PSC-PWM resulted in 30.6% and 30.9% voltage and current THDs, respectively. It also causes non-uniform voltage stress on the switching devices. For high power factor operation, the voltage ripples in flying capacitors are also higher, which proves the PSC-PWM has poor performance in comparison with PD-PWM at steady state operation. Overall, it is observed that both PD-PWM and PSC-PWM schemes are incapable of regulating the flying capacitor's voltage at higher power factors and modulation indices.

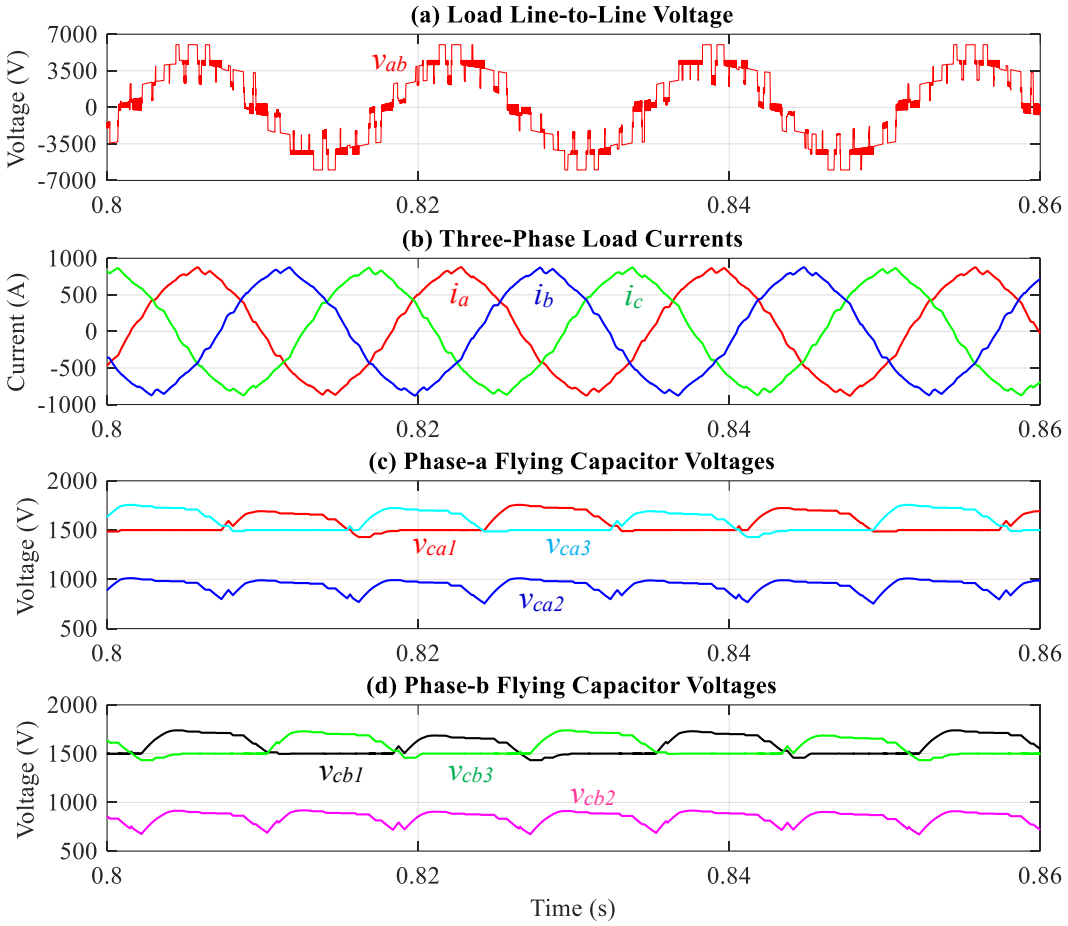


Fig. 4.3: Steady-state performance at a power factor of 0.85 (lag).

4.2.2 Transient Performance:

The performance of the voltage balancing method with the PSC-PWM under step-change in modulation index from 0.4 to 0.9 is shown in Fig. 4.4. The load power factor is set to 0.55 (lag). When the modulation index is 0.4, the inverter generates a voltage waveform with five steps and has a THD of 63.62% as shown in Fig. 4.4(a). The load currents are sinusoidal and have a THD of 3.90% as shown in Fig. 4.4(b). The flying capacitor voltages of phase-a and phase-b are maintained at 1500 V as shown in Fig. 4.4(c) and 4.4(d), respectively. These capacitors have a ripple of 249 V (peak-to-peak). With the rise in the modulation index from 0.4 to 0.9, the number of steps in the output voltage and the current magnitude is also increased. This increment leads to a lower THD in the voltage and current of 25.32% and 1.77%. Also, the flying capacitor voltage ripples are increased to 408 V due to the rise in the current magnitude as shown in Fig. 4.4.

Irrespective of the external disturbance, the flying capacitor voltages are regulated close to their rated values.

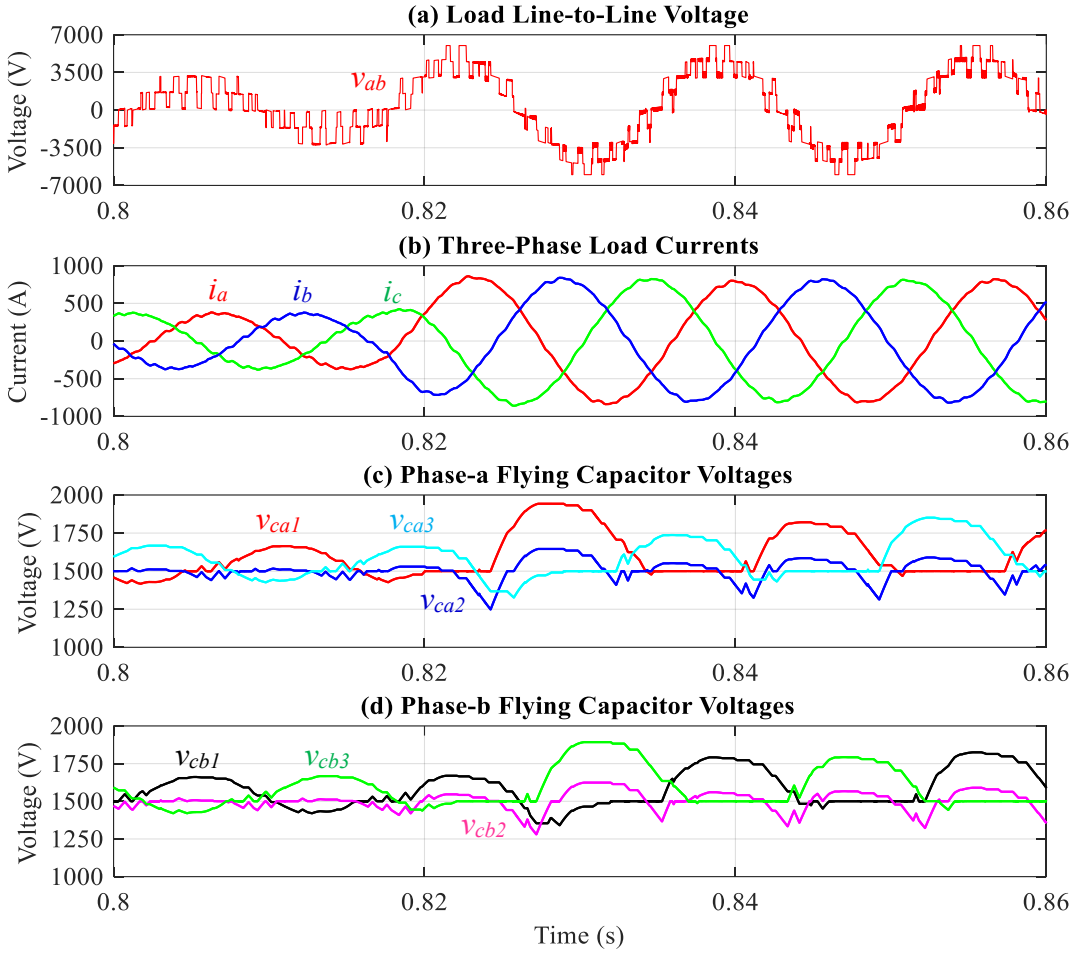


Fig. 4.4: Transient performance.

4.2.3 Performance Analysis:

Fig. 4.5 depicts the performance analysis of the five-level MLI with the PSC-PWM and its comparison with the PD-PWM scheme. The voltage THD and current THD decrease with the rise in the modulation when the MLI is modulated with the PSC-PWM scheme as shown in Figs. 4.5(a) and 4.5(b), respectively. The PD-PWM scheme has less harmonics in most operating conditions compared to PSC-PWM, except between a range of 0.5 to 0.7 modulation index. The harmonics showed close results for both PD-PWM and PSC-PWM at this operating range of 0.5 to 0.7 modulation index. On the other hand, the flying capacitor voltage ripples increase with the modulation index due to the rise in

the load current magnitude as shown in Fig. 4.5(c). The ripple increase for PSC-PWM is more similar to the ripple increase in PD-PWM. Furthermore, these ripples are well above the set limits of 10% of the rated value. Although the harmonics of PSC-PWM satisfies IEEE-519 standards, it is also observed that the PSC-PWM has poor harmonic performance compared with the PD-PWM, whereas the voltage ripple performance is very close to each other.

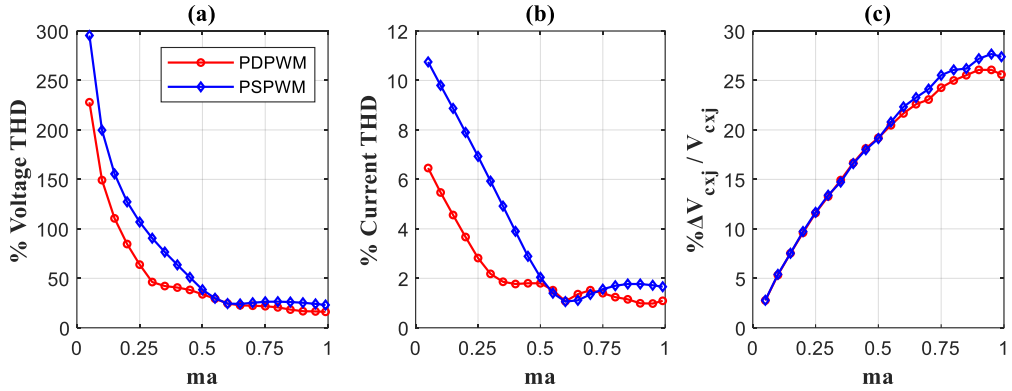


Fig. 4.5: Performance analysis at a power factor of 0.55 (lag): (a) voltage harmonic distortion (%V_{THD}), (b) current harmonic distortion (%I_{THD}), and (c) Flying capacitor voltage ripple (%ΔV_{Cxj} /V_{Cxj}).

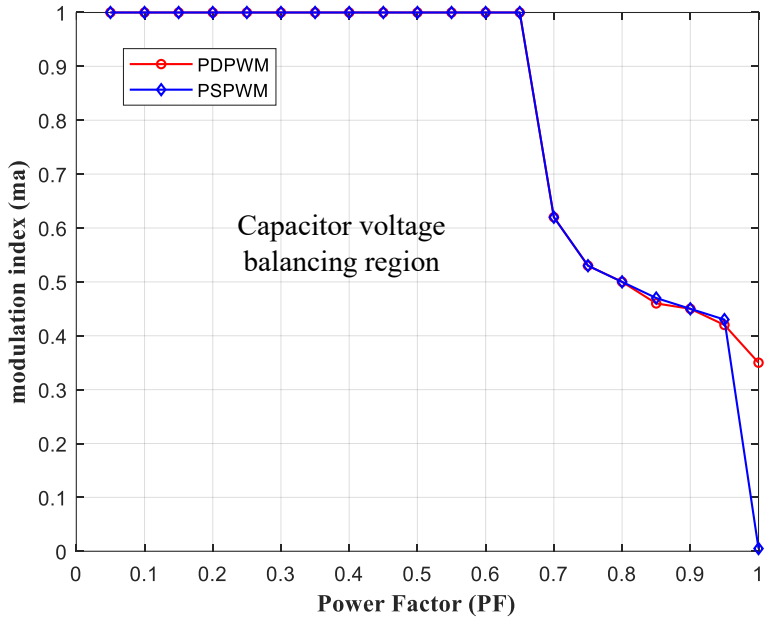


Fig. 4.6: Voltage balancing boundary limits of PD-PWM and PSC-PWM.

4.2.4 Voltage Balancing Boundary Limits:

Fig. 4.6 depicts the capacitor voltage balancing limits of the PSC-PWM and its comparison with the PD-PWM scheme. The PSC-PWM scheme ensures the flying capacitor's voltage balancing up to a power factor of 0.65 when the modulation index is unity. As the power factor increases, the modulation index should be lowered to achieve voltage balancing in the five-level MLI. This performance is similar to the PD-PWM scheme performance as shown in Fig. 4.6. It is also noted that the unity power factor operation is not feasible with the PSC-PWM.

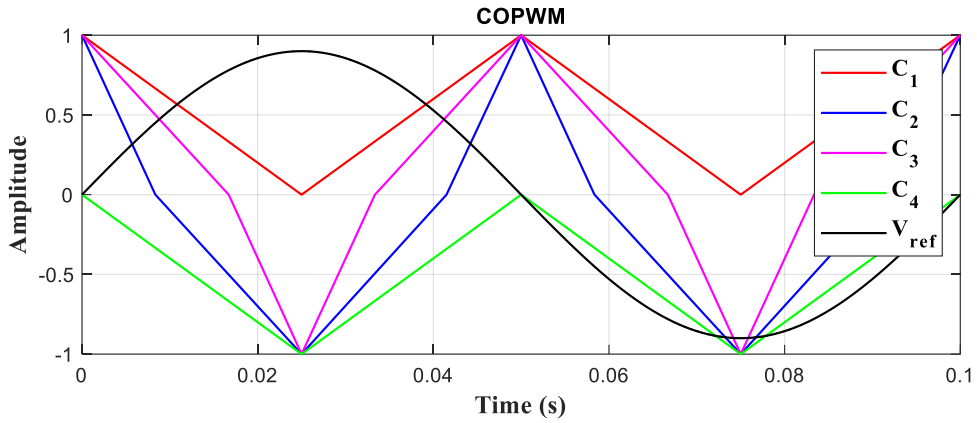


Fig. 4.7: Carrier arrangement in the COPWM scheme,

4.3 Modified PD-PWM Scheme:

The triangular carrier signals are uniformly disposed of vertically in the PD-PWM, whereas they are disposed of horizontally in the PSC-PWM scheme. However, the uniform disposition of the triangular signals is unable to regulate the flying capacitor's voltage at higher power factors and modulation indices. Furthermore, these methods cause higher capacitor voltage ripple of more than 10%. Considering these issues, the non-uniform disposition of triangular carrier signals is considered in this study. In addition, from the charge balance analysis, the middle voltage levels have an unbalanced effect on the flying capacitor's voltage. Therefore, the middle triangular carriers in the conventional PD-PWM scheme are rearranged to form the modified carrier overlap PWM (COPWM) scheme.

The carrier arrangement in the COPWM scheme is shown in Fig. 4.7. This method divides the carrier space into two regions named upper carrier region and lower carrier region. The uppermost and lowermost carrier signals occupy their respective carrier region completely. On the other hand, the middle two carriers cover the entire carrier space as illustrated in Fig. 4.7. These middle carriers have twice the magnitude of other carrier signals. There are numerous possible ways of middle carriers arrangement have been studied in literature but the arrangement here is made considering that zero-crossing of all carriers are equally distributed. This makes a standard pattern of arrangement for the carriers. The carrier signals are compared with the modulation signal and resultant comparison outputs are added together to form a normalized output voltage waveform. This normalized five-level voltage waveform will have overlapping voltage steps as opposed to the symmetrical steps in the conventional PD-PWM scheme. The normalized output voltage is used with the voltage balancing method shown in Fig. 3.8 to control the flying capacitor's voltage.

4.4 SIMULATION STUDIES:

The voltage balancing ability of the COPWM scheme is verified on a 5 MVA/4.16 kV rated five-level MLI using MATLAB simulation tools. In this study, the system's DC-bus voltage is set to 6000 V. Each flying capacitor is designed with a capacitance of 3000 μF and a voltage rating of 1500 V. The passive load parameters are adjusted to achieve the required lagging power factor operation. The triangular carrier signals are generated with a frequency of 1000 Hz so that the equivalent switching frequency of the MLI is equal to the conventional PD-PWM scheme.

4.4.1 Steady-state Performance:

The steady-state performance of the voltage balancing method with the COPWM at a load power factor of 0.55 (lag) is shown in Fig. 4.8. In this study, the modulation signals are generated at a modulation index of 0.99 and a frequency of 60 Hz. Due to the non-uniform disposition of triangular carrier signals, the output voltage steps are not symmetrical and have overlapped features as shown in Fig. 4.8(a). The voltage has a THD of 38.96%. The overlapped voltage steps led to a higher ripple in the load current compared with the conventional PD-PWM as shown in Fig. 4.8(b). The load current has a THD of 2.20%. The flying capacitor voltages of phase-a and phase-b are perfectly

regulated at their rated values of 1500 V as shown in Figs. 4.8(c) and 4.8(d), respectively. The charging and discharging process of the flying capacitors C_{x1}, C_{x2}, and C_{x3} follow the charge balance principle. In terms of neutral-point currents i_{Nx1} and i_{Nx2}, they have equal magnitudes and are opposite in phase. Therefore, the capacitor C_{x1} is charging while the capacitor C_{x3} is discharging. These capacitors have a voltage ripple of 235 V (p-p). On the other hand, the capacitor C_{x2} voltage is perfectly regulated at its rated value without any ripple.

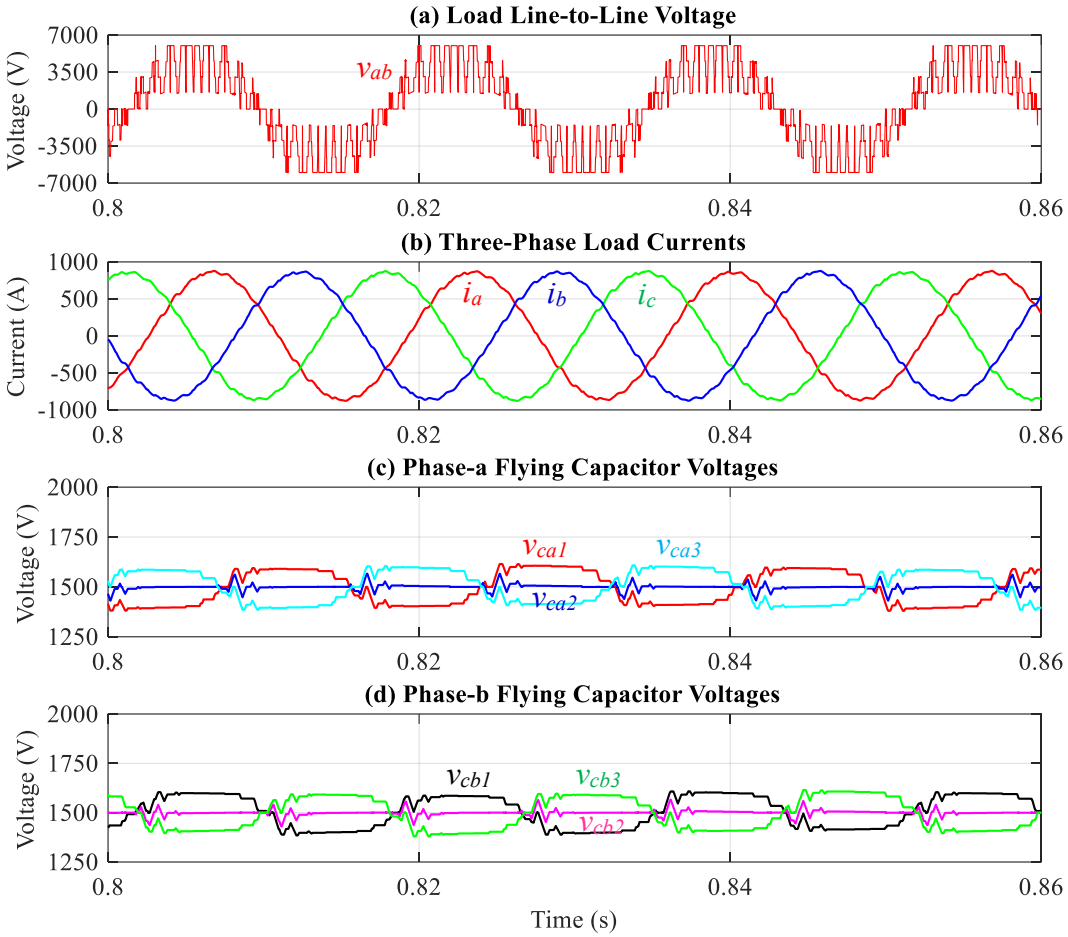


Fig. 4.8: Steady-state performance at a power factor of 0.55 (lag).

The simulation studies are extended to the higher power factor operation of 0.85 (lag) and the corresponding results are shown in Fig. 4.9. The output voltage has overlapped voltage steps, which is similar to the low power factor operation leading to a THD of 39.1% as shown in Fig. 4.9(a). The load currents have a THD of 3.47%, which is well below the 5% limits as per the IEEE-519 standard as shown in Fig. 4.9(b). The

flying capacitor voltages of phase-a and phase-b are regulated at their rated values of 1500 V as shown in Figs. 4.9(c) and 4.9(d), respectively. Also, these capacitors have a ripple of 165 V. Even though the COPWM causes higher harmonic distortion in the output voltage and current, it is still able to minimize the flying capacitor voltage ripple compared with the conventional PD-PWM scheme. Also, the COPWM scheme guarantees the flying capacitor's voltage regulation at higher power factors and modulation indices compared with the conventional PD-PWM scheme.

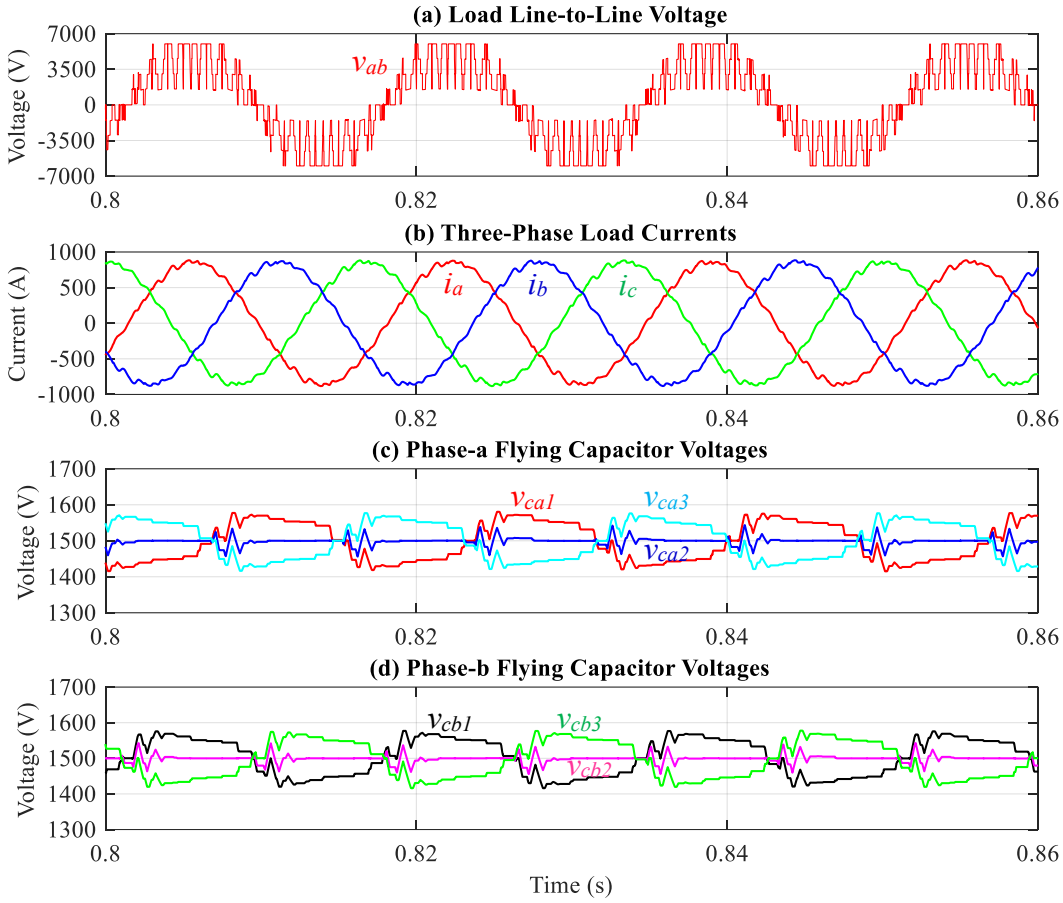


Fig. 4.9: Steady-state performance at a power factor of 0.85 (lag).

4.4.2 Transient Performance:

The transient performance of the COPWM scheme with the step-change in the modulation index from 0.4 to 0.9 is shown in Fig. 4.10. At 0.4 modulation index operation, the MLI generates voltage waveform with symmetrical steps as shown in Fig. 4.10(a). The output voltage has a THD of 44.99%. The load draws balanced load currents

with a THD of 1.43% as shown in Fig. 4.10(b). Each flying capacitor voltage in phase-a and phase-b is maintained at 1500 V as shown in Figs. 4.10(c) and 4.10(d), respectively. The capacitors C_{x1} and C_{x3} have a voltage ripple of 120 V peak-to-peak. As the modulation index is increased to 0.9, the number of steps in the output voltage is also increased, leading to a reduction in the THD to 42.27% as shown in Fig. 4.10(a). This reduction is much smaller due to the overlapped steps in the output voltage. Also, the current magnitude increased to 920 A and has a THD of 2.02% as shown in Fig. 4.10(b). The flying capacitor voltages are still maintained at their rated values. However, the voltage ripples are increased to 218 V peak-to-peak as shown in Figs. 4.10(c) and 4.10(d). Overall, the COPWM effectively regulates each flying capacitor voltage at 1500 V irrespective of the external disturbance.

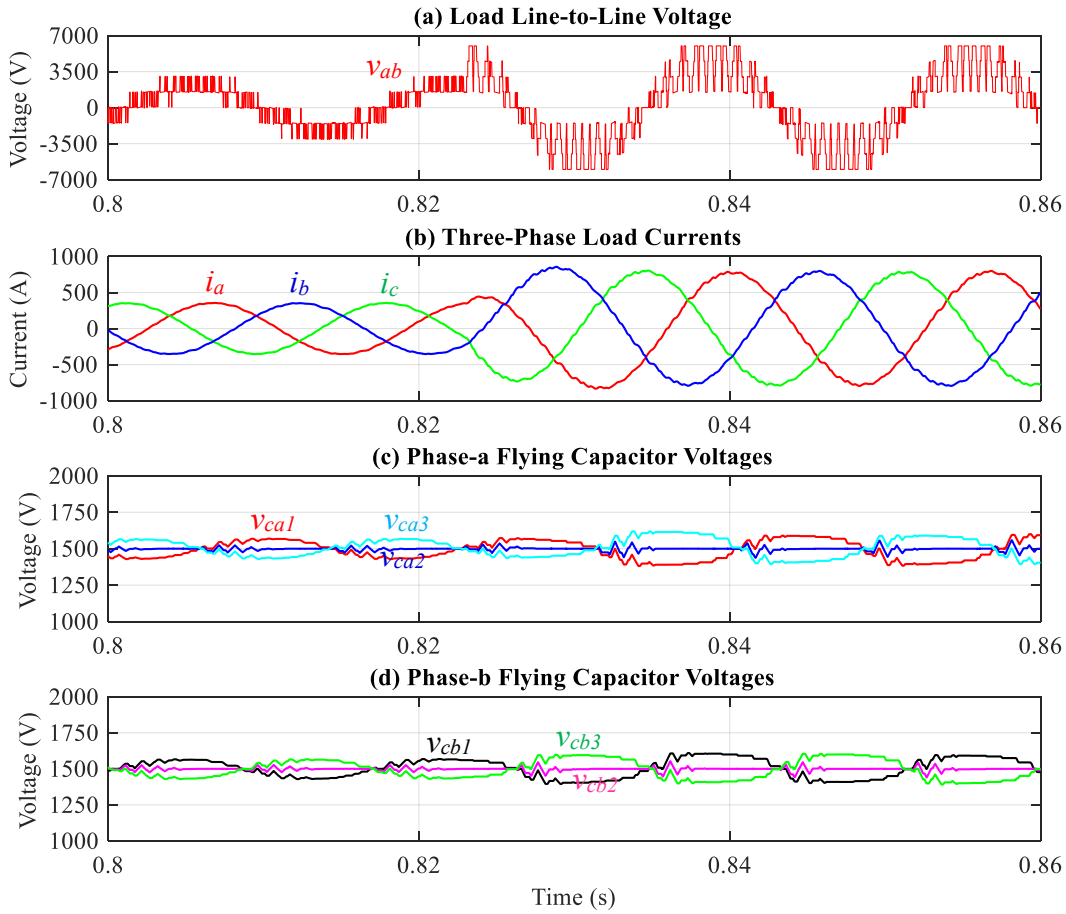


Fig. 4.10: Transient performance analysis.

A summary of the PD-PWM, PSC-PWM and COPWM schemes is presented in Table 4.1. It is observed that the PD-PWM scheme has superior harmonic performance compared with the PSC-PWM and COPWM schemes. However, it causes a higher-flying capacitor voltage ripple. On the other hand, the COPWM causes less voltage ripple in the flying capacitors at the cost of higher harmonic distortion in the current and voltage waveforms compared with the PD-PWM. The PSC-PWM has poor performance in terms of voltage ripple and THDs compared with the PD-PWM scheme.

Table 4.1: Comparison of multicarrier PWM schemes

Parameter	PF=0.55, m_a = 0.99 and f_o=60Hz		
	PD-PWM	PSC-PWM	COPWM
$\%V_{rip}$	25.6	27.4	15.6
$\%V_{THD}$	16.15	23.05	38.96
$\%I_{THD}$	1.09	1.66	2.20

4.4.3 Performance Analysis:

The performance of the COPWM is further analyzed at different modulation indices and compared with the PD-PWM and PSC-PWM schemes. It is observed that the voltage THD with the COPWM scheme is comparable to the PD-PWM performance up to a modulation index of 0.5. For the above 0.5 modulation index, the voltage THD becomes worse compared with the PD-PWM and PSC-PWM schemes as shown in Fig. 4.11(a). The current THD with COPWM also follows the same pattern of the voltage THD as shown in Fig. 4.11(b). On the other hand, the capacitor voltage ripple with COPWM is much lower compared with other PWM schemes. However, these ripples are well above the design limit of 10% ripples.

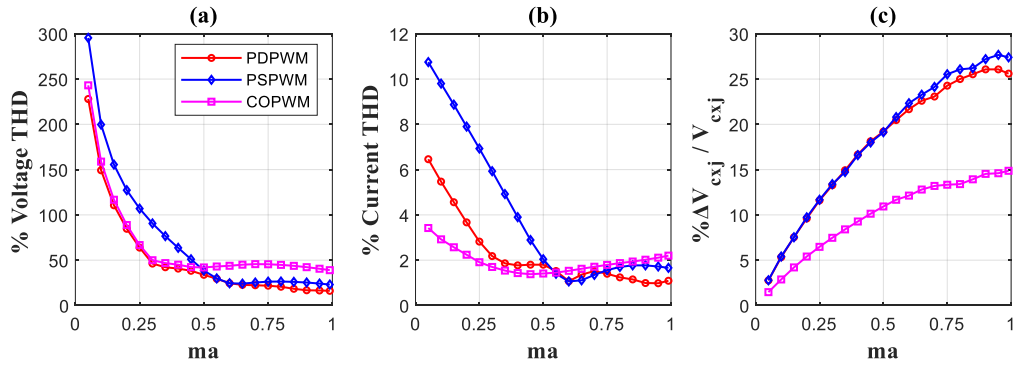


Fig. 4.11: Performance analysis at a power factor of 0.55 (lag): (a) voltage harmonic distortion (%V_{THD}), (b) current harmonic distortion (%I_{THD}), and (c) Flying capacitor voltage ripple (%ΔV_{Cxj} /V_{Cxj}).

4.4.4 Voltage Balancing Boundary Limits:

Fig. 4.12 depicts the voltage balancing boundary limits of the COPWM scheme. It is observed that the COPWM can regulate the flying capacitor's voltage at its rated value even under higher power factors and modulation indices compared with the PD-PWM and PSC-PWM schemes. Hence, the COPWM will be a suitable candidate to control the five-level MLI under a wide range of operating conditions.

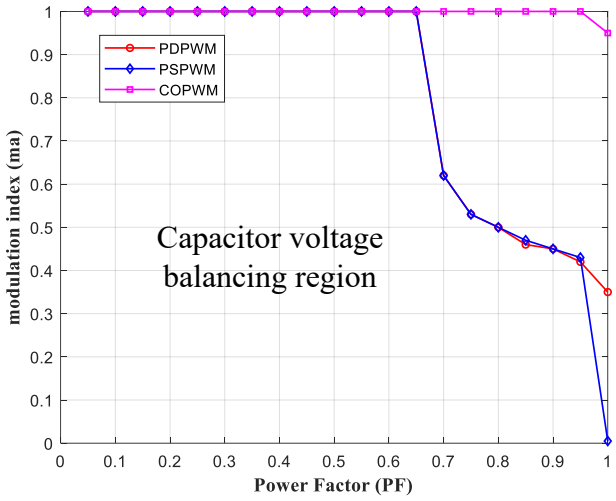


Fig. 4.12: Voltage balancing boundary limits of PD-PWM, PSC-PWM, and COPWM.

4.5. Summary:

In this chapter, the modified multicarrier PWM schemes including PSC-PWM and COPWM schemes are investigated for the five-level MLIs. It is observed that the PSC-PWM is unable to control the flying capacitor's voltage at higher power factors. Furthermore, it has poor harmonic performance and higher capacitor voltage ripple compared with the PD-PWM scheme. On the other hand, the COPWM can control the voltage of the flying capacitors irrespective of the power factor and modulation index. In addition, it has the lowest flying capacitor voltage ripple compared with the PD-PWM and PSC-PWM schemes. Also, the COPWM has comparable harmonic performance up to a modulation index of 0.5 solely. For above 0.5, it has poor harmonic performance compared with the PD-PWM and PSC-PWM schemes.

CHAPTER 5

CONCLUSIONS

This thesis addresses the voltage balancing issues in a new five-level MLI with the multicarrier PWM schemes. The thesis introduces a Five-Level MLI for medium voltage applications. The topology has a smaller number of devices and reduced control complexity in comparison with the other conventional MLIs. A voltage balancing approach was developed for the Five-level MLI and its performance is analysed with multicarrier modulation schemes. A modified carrier PWM scheme was developed to control FC voltages even under higher power factor operations. Also, the FC voltage ripples are minimized with this modified carrier PWM scheme. However, it has higher harmonic distortion compared with IPD-PWM and PSC-PWM, it had wide operating region suitable foe grid and motor systems. Overall, the modified carrier PWM scheme was found to be the best candidate to control the developed five-level MLI at high power factor and modulation indices.

The present work comprises topology and operation of five-level MLI, theoretical analysis and mathematical modelling of the flying capacitor's voltage, development of voltage balancing method, and performance analysis of multicarrier PWM schemes.

5.1 CONTRIBUTIONS:

The contributions of this thesis are summarized as follows:

1) A new five-level MLI with a reduced component count for medium-voltage applications

The component count and control complexity are the major issues in the conventional five-level MLIs. Also, some of the topologies require a phase-shift transformer to generate isolated DC sources. To overcome these problems, a new five-level MLI with a reduced component count is introduced. Also, the new MLI does not require isolated DC sources and the corresponding phase-shift transformer as well. In addition, the control complexity is relatively low. However, the reliability of the new MLI is poor due to its integrated structure.

2) A generalized structure of the voltage balancing method for the five-level MLI

The flying capacitor's voltage balancing is a key control objective to achieve a five-level operation in the new MLI. The flying capacitor's voltage variation is analyzed theoretically and mathematically using the charge balance principle. Finally, a generalized structure of the voltage balancing method for the five-level MLI is introduced.

3) Investigation of voltage balancing performance with the multicarrier PWM schemes

The performance of the voltage balancing method with the conventional PD-PWM and PSC-PWM schemes is verified using MATLAB simulations. The results show that the PD-PWM scheme has a superior harmonic performance compared with the PSC-PWM. However, these methods are unable to control the flying capacitor's voltage for the load power factors above 0.65 at the unity modulation index. To overcome this problem, a carrier overlapped PWM (COPWM) scheme is introduced. The COPWM effectively regulates the flying capacitor's voltage irrespective of the operating scenarios. Also, it causes less voltage ripple in the flying capacitors. However, the COPWM has poor harmonic performance for above 0.5 modulation index compared with the conventional PD-PWM.

5.2 FUTURE WORK:

The present study shows that the COPWM can balance the flying capacitor's voltage with less ripple at all power factors, but at the expense of higher harmonic distortion. Furthermore, the studies are conducted by varying the pattern of the triangular signals only, but it is also possible to modify the modulation signals to handle the voltage balancing issues in the MLI. Also, the performance analysis is verified at different load power factors only. Considering these aspects, the following works are suggested for future research:

- Further investigation of the COPWM scheme is necessary to improve the harmonic performance.
- The voltage balancing analysis with the change in the modulation signals pattern rather than carrier signals pattern.

- Performance analysis at different output frequencies so that it can be applied to electrical machine applications.
- Experimental verification of the proposed methods through the laboratory prototype.

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